

A Novel Architecture for Switched-Capacitor FIR Filters

by

Syed Tauseef Nizam Ahmed

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

December, 1995

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Syed Tauseef Nizam Ahmed

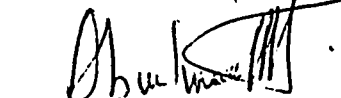
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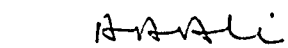
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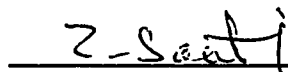
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Dedicated to

my parents

ℰ

my brothers and sisters

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Abstract

Name: Syed Tauseef Nizam Ahmed
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This thesis describes the complete design procedure for switched-capacitor filters that can accept both analog and digital signals. These filters are characterized by the fact that the same filter structure can be used to obtain any desired filter response. The filters can be made programmable as well as adaptive.

The complete integrated circuit implementation of an 8th and a 16th order SC filters are done using SCMOS technology. CaZM simulation results of all the basic building blocks are also presented.

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هذه الأطروحة تبين طريقة تصميم مرشحات ذات مكثفات متغيرة Switched- Capacitor (SC) . والتي تُستعمل للإشارات التماثلية والرقمية .

وهذه المرشحات مميزة بخيـث نفس البنية يمكن أن تكون مبرمجة كما يمكن أن تكون متعددة الاستعمال

الدائرة المتكاملة لمرشحين SC من الدرجتين 8 و 16 تم إنجازها باستعمال تكنولوجيا SC MOS . كذلك النتائج المحصل عليها باستعمال محاكاة لكل الطبقات المكونة للمرشح مبينة .

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Chapter 1

Introduction

Continuous analog circuits consist of resistors, capacitors and active elements, besides other components. The performance of these circuits therefore depend upon the accuracy of these components. Also large time constant circuits require large value of resistances which in turn require large areas on the chip, in addition to being temperature dependant. These factors therefore discourage the use of such components in IC chips. An alternative approach is the switched-capacitor (SC) technique, where the circuit performance depends on the capacitor ratios. Since the latter can be fabricated to within an accuracy of 0.1 %, the resulting circuits are extremely precise.

Over the last decade the literature on switched-capacitor circuits has boomed a lot. Most of the papers describe non programmable SC filters. This thesis describes in detail the design procedure for a programmable SC FIR filter. The main feature

of the design is that it can accept both analog and digital signals.

1.1 Thesis outline

In chapter 2 we give a brief review of SC circuit design, then study the FIR and IIR structures in general. We show the history of SC circuit theory, and how it has developed into today's widely used exact SC circuit design. Analysis of IIR and FIR structures is presented and it is shown that the FIR is more suitable for the programmable applications. The architecture of the programmable SC FIR filter is described and the main features of the architecture are discussed.

The design considerations in MOS integrated circuits are discussed in chapter 3. The complete IC design of an unbuffered CMOS operational amplifier is given and the simulation results are presented. Some configurations of the switch and the capacitor are presented and analyzed.

The integrated circuit design and simulation results of each block of the programmable filter are shown in chapter 4. This chapter also describes the causes of imperfections in the building blocks and suggests solutions to optimize the performance. Chapter 4 also shows the complete IC design of an 8th and 16th order programmable FIR filters. The simulation results are also presented and discussed.

Chapter 2

Overview of Switched Capacitor and FIR Filters

Over the past fifteen years, switched-capacitor filters have emerged from the state of curiosity to a well established filtering technique that has found widespread application in the communications industry. In this chapter, a historical background of SC circuit design will be given, starting from the very primitive approximate circuit designs to the more complex exact solutions used today.

2.1 Switched-Capacitor Circuits and the IC Technology

Switched-capacitor circuits are advantageous only in an integrated circuit implementation. An equivalent analog continuous-time circuit has less components, and is simpler than its SC counterpart. However, continuous time analog circuits with resistors and capacitors have their limitations when implemented on an IC chip. Their problems are the sizes, and the inaccuracies of the passive components. Passive resistors on an IC have a limited resistance range and a poor accuracy, besides occupying large chip areas. They are also temperature and voltage dependant and are therefore unsuitable for integration.

The performance of switched-capacitor circuits depends upon capacitor ratios. Since these ratios can be controlled to within an accuracy of 0.1% [1], the resulting circuits are extremely precise. Therefore high performance integrated circuits can be obtained. However, there are two major drawbacks in the IC implementation of SC circuits. One is the existence of noise, and the other, is the existence of parasitic capacitances.

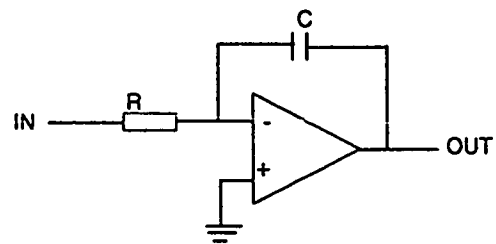
IC's are fabricated in layers. Semiconductor, insulator and conductor layers are put together to construct the various devices such as transistors, capacitors etc. These layers have some amount of capacitance between each other, and these parasitic capacitances are in the same order of magnitude as the desired capacitor itself.

Since SC circuits operate by transferring charge between capacitors, the existence of parasitic capacitances does effect this transfer. Therefore design engineers have to make parasitic insensitive circuits to overcome this problem.

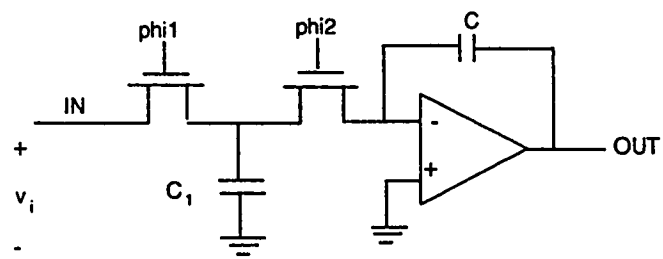
SC circuits are widely used in the telecommunications industry. They are used to manufacture precision analog circuits.

2.2 The Evolution of SC Filter Design

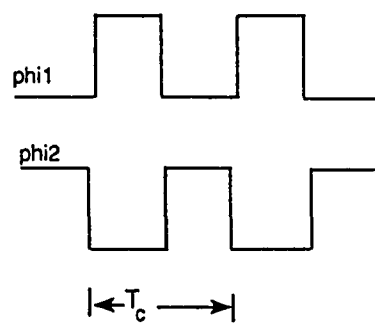
High quality analog filters were historically realized as passive LCR circuits. Since inductors are physically large, electrically lossy and noisy, they are unsuitable for miniaturization. An effort to replace them began in the 1960's. The resulting circuits were the active RC filters which were widely used for the next twenty years. However, the straightforward integration of an active RC filter leads to difficulties. Since integrated filters are commonly used in the audio range, they require time constants of the order of $10^{-4}s$. Even for a capacitor of $10pF$, a resistor of the order of 10^7 has to be used. Such a resistor requires a chip area of around $10^6\mu m^2$, or nearly 10% of the total chip area [2]. In addition to this, MOS resistors tend to be non linear and also temperature dependant. As a result the overall error of an RC time constant can be 20% [3]. To overcome these difficulties, *simulated resistors* were constructed from capacitors and switches [4].



(a)



(b)



(c)

Figure 2.1: (a)Continuous Euler Integrator (b)Bilinear SC Integrator (c) Two-phase-clock

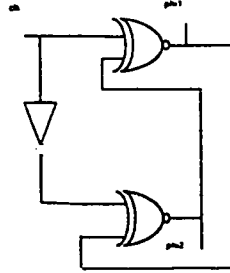


Figure 2.2: Circuit to obtain a two-phase clock

2.2.1 The Equivalent Resistor approach

In its early stages, the switched-capacitor technique was based on the realization that a capacitor switched between two circuit nodes at a sufficiently high rate is equivalent to a resistor connecting these two nodes.

Consider the RC integrator shown in Figure 2.1(a). In Figure 2.1(b) the resistor R is replaced by a grounded capacitor C_1 together with two MOS transistors acting as switches. The switches are driven by a *non overlapping* two-phase clock. The circuit diagram of a two phase clock generator are shown in Figure 2.2. It has two output signals $\phi1$ and $\phi2$, which are non-overlapping. The clock frequency f_c is kept much higher than the frequency of the signal being filtered.

The operation of the circuit is as follows: During $\phi1$, when $C1$ is connected across the signal v_i , the variations in the input signal are negligibly small. Therefore during $\phi1$ the capacitor C_1 charges up to the voltage v_i .

$$qC_1 = C_1 v_i$$

Then, during the clock phase $\phi2$, capacitor C_1 is connected to the virtual ground of

the op amp. The Capacitor C_1 is thus forced to discharge and its previous charge qC_1 is transferred to C

Thus, during each clock period T_c an amount of charge $qC_1 = C_1 v_i$ is extracted from the input source and supplied to the integrator capacitor C thus the average current flowing between the input node and the virtual ground of the op amp is

$$i_{av} = \frac{C_1 v_i}{T_c}$$

If T_c is sufficiently short, one can assume the process to be as almost continuous and define an equivalent resistance R_{eq} that is effectively present between the input node and virtual ground of the op amp.

$$R_{eq} = T_c / C_1$$

The equivalent time constant for the integrator is

$$R_{eq}C = T_c \frac{C}{C_1}$$

The time constant is thus determined by the clock period T_c , and the capacitor ratio C/C_1 . The accuracy of capacitor ratios in MOS technology can be controlled to within 0.1%

Therefore we have an SC circuit that can be used to replace a resistor. This configuration however, is sensitive to stray capacitances.

Switched-Capacitor Integrators

The basic building block of active RC filters is the active RC integrator shown in Figure 2.1(a). Its input output relation is

$$v_o(t) = -\frac{1}{RC} \int v_i dt$$

or, in the Laplace-transform domain,

$$V_o(s) = -\frac{V_i(s)}{sRC}$$

Replacing R by a simulated resistor, the circuit in Figure 2.1(b) results.

To obtain the exact expression for R_{eq} , we can observe that at $t = t_{n-1}$ the capacitor C_1 charges to $v_i(t_{n-1})$ and acquires $C_1 v_i$ charge. At $t = t_{n-1} + T_c/2$, this new charge has been added to the charge already stored in C , and the new charge is held. Hence at $t = t_n$ the output voltage is

$$v_o t_n = v_o t_{n-1} - \frac{C_1}{C} v_i(t_{n-1})$$

Using Z transform to solve this difference equation results in the transfer function

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C} z^{-1} / (1 - z^{-1})$$

Therefore the replacement of all RC integrators in an active RC circuit by an SC circuit is equivalent to replacing s by $(z - 1)/T_c$. This is known as forward-difference-mapping [3] which is used in the design of digital filters from an analog model.

The effects of stray capacitances can be eliminated by using the stray insensitive configuration shown in Figure 2.3. In this circuit, the capacitor C is periodically

charged to the input voltage V_i . For an ideal op amp, none of the stray capacitances contribute to the charge in capacitor C_2 . The reason for this insensitivity is that every capacitor terminal is switched between low- impedance nodes (i.e. Physical ground and an op amp output) or is switched between ground and virtual ground. Hence none of them effect the output.

The simplest design technique for SC filters would be to replace all resistors in the analog realization, with switched capacitor resistors. Two examples of this technique are shown in Figure 2.3

The output of the inverting and non-inverting integrators are given as,

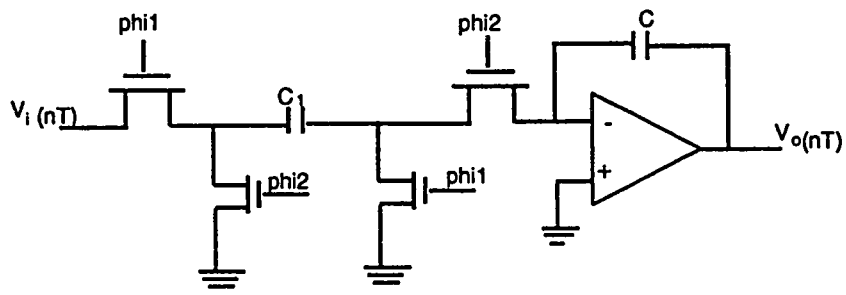
$$V_o(nT) = V_o((n-1)T) - \frac{C_1}{C_f} V_i(nT)$$

$$V_o(nT) = V_o((n-1)T) + \frac{C_1}{C_f} V_i(nT)$$

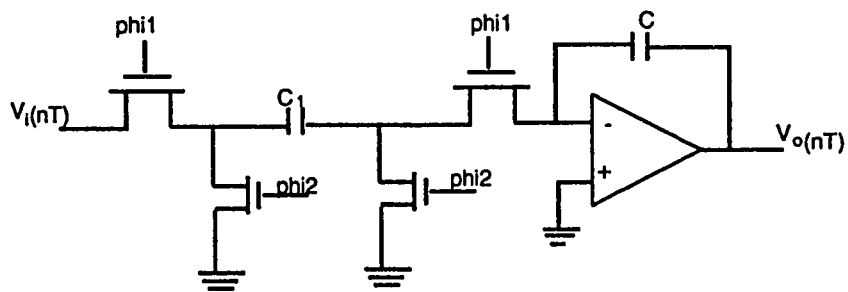
respectively.

Switched-capacitor biquad filters can be constructed using these basic blocks. Due to the use of SC resistors, the clock frequency in these filters has to be much higher than the band limit frequency of the signal f_{max} , which is a major disadvantage. Usually $f_{clock} > 50f_{max}$ [5].

This technique is no more utilized in SC filter design because of its disadvantages in comparison with the exact filter designs.



(a)



(b)

Figure 2.3: (a) Non-inverting SC Integrator (b) Inverting SC Integrator

2.2.2 The Ladder Filters

The simplest design technique for SC filters is to replace all resistance in an active RC prototype circuit by switched capacitors. This approach was followed for constructing integrators and first and second order sections. By cascading such sections, higher order filters can be realized. However, the element value sensitivities becomes a problem. If the passive filter has a ladder configuration, then the sensitivities will be low compared to the cascade realization [3]. For active RC filters, the approach followed to obtain the final circuit from its passive model is usually component simulation. This approach was also adopted for SC filter design [6]. However, the resulting structures were not widely used for commercial applications due to their sensitivity to parasitic capacitances. The N-path filter was also one of the early architectures used for SC filters. It is made of N low-pass/high-pass filters in parallel, switched into the circuit sequentially so that one system is connected at a time. This structure permits the realization of narrow band-pass/band-reject filters on the basis of low-pass/high-pass filters. The frequency response of the N-path filter is defined by the cutoff frequency f_c of the low-pass/high-pass, the number of parallel elements N and the switching frequency f_{clk} as follows:

$$f_o = \frac{f_{clk}}{N}$$

$$BW = 2 \frac{f_{clk}}{N}$$

where f_o is the center frequency and BW the bandwidth of the filter. The frequency of this system depends only on the clock frequency and the number of elements; therefore it is independent of the element value variations [7].

Another popular approach to the active RC filter design is based on the signal flow graph representation (SFG) [8] of the current voltage relations of the passive model. The active RC filter is designed as an analog computer realizing the SFG such that the op amp output voltages represent the node voltages and the branch currents. This design technique is not used extensively for high order RC filters, since the number of op amps required is equal to the order of the filter. Also, many resistors are needed in the circuit. However, the SFG strategy is suitable for integrated filters, which can result in high order, high accuracy switched-capacitor filters [9, 10]. SC ladder filters were historically designed using approximate techniques where the clock frequency has to be much larger than the signal frequency.

2.3 The Exact SC Filter Design

In the early 80's the exact solution to the SC filters was developed, which uses a completely different approach to the problem. Due to the substitution of the resistor, the early design techniques relied on very high sampling rates and an analog prototype. The exact techniques use either the loss-less discrete integrator (LDI) [11] or the bilinear transformation [12, 13, 14]. The LDI ladder filters are characterized

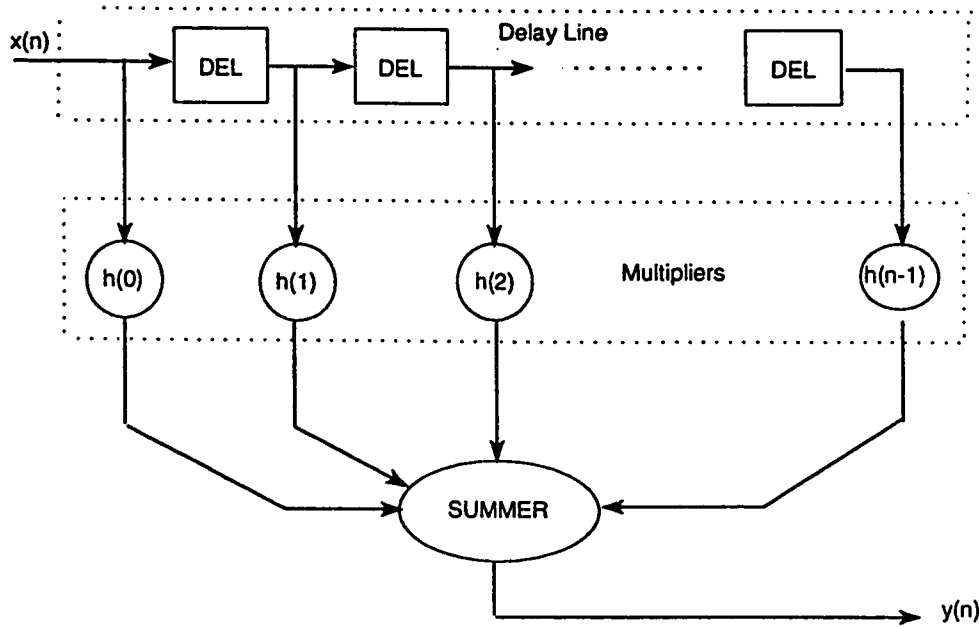


Figure 2.4: FIR Filter Block Diagram

by their low-sensitivity to element value variations. These filters have no lumped-element counterparts, and therefore a complete synthesis technique is necessary for their design.

2.3.1 The SC FIR filter

An SC filter can be constructed based on the digital filter architecture, by constructing SC versions of the basic elements of a digital filter. These basic elements are delay lines, multipliers and adders. An example of the structure of a digital filter is shown in Figure 2.4

The advantage of using the digital filter architecture is that much of the research

done on the digital filters can also be used for the SC filter. For example, filter design, adaptive algorithms, and effects of imperfections in the system, have been already studied and in many cases could be directly applied to the digital filters, due to their similar architectures.

2.4 The IIR and FIR filters

In general filters can be classified as either *finite impulse response* (FIR) or *infinite impulse response* (IIR). Each configuration has its own advantages and it is up to the designer to decide whether one or the other configuration is more suitable for the application. This section shows FIR and IIR structures, and discusses the advantages and disadvantages of both types.

2.4.1 The IIR Structure

This filter is characterized by an output that consists of a linear combination of present value of the input and past values of the output as shown by

$$y(n) = x(n) + \sum_{k=1}^M a_k y(n - k)$$

where $x(n)$ is the present value of the filter input; $y(n)$ is the present value of the filter output; $y(n - 1)$, $y(n - 2)$, ..., $y(n - M)$ are the past values of the filter output. The signal flow graph representation of the filter is described in Figure 2.5b. The

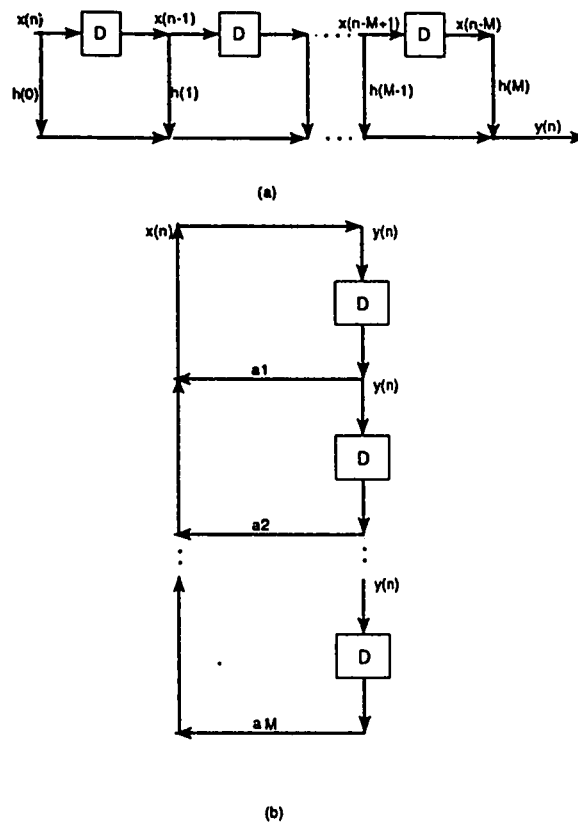


Figure 2.5: Signal-flow-graph representations of (a) FIR filter, and (b) IIR filter

design of the IIR filter is the approximated by the rational function

$$H_{IIR}(z) = \frac{\sum_{k=0}^M b_k z^{-k}}{\sum_{k=0}^N a_k z^{-k}}$$

There are closed form design formulas to calculate the coefficients of the filter, given the filter specifications and type. However this facility of the filter design is limited to the most common basic filter configurations, like low-pass, high-pass, band-pass and band-reject. If arbitrary frequency response is desired, the filter design problem becomes rather difficult.

2.4.2 The FIR Structure

This filter is characterized by an output that consists of a linear combination of present and past values of the input. Let $x(n)$ denote the present value of the input, and let $x(n-1), x(n-2), \dots, x(n-M)$ denote the M past values of the input. Let $y(n)$ denote the present value of the filter output. The input-output relation of the filter is described by the convolution sum [15]

$$y(n) = \sum_{k=0}^M h(k)x(n-k).$$

The impulse response of a discrete time filter is defined as a filter output produced by an input that consists of a unit pulse sequence. Hence the impulse response of the filter equals the sequence of filter coefficients $h(0), h(1), \dots, h(M)$. Since this sequence is of finite duration for a prescribed M , the filter is referred to as a *finite*

impulse response filter. To design an FIR filter the desired frequency response is approximated by the polynomial [15],

$$H_{FIR}(z) = \sum_{n=0}^{N-1} h_n z^{-n}$$

The phase response of the FIR filter can be made exactly linear by forcing the impulse response to be symmetric or anti-symmetric. Also the FIR filter is unconditionally stable, since it has no poles in its transfer function.

The FIR filter is a very attractive structure for adaptive systems due to its simple and unconditionally stable structure. A wide variety of adaptive algorithms have been developed for the FIR filter that can be applied directly to the SC FIR filter.

Using the FIR filter, any arbitrary filter response specifications can be implemented with a little more effort than is necessary for the design of low-pass filter, and once the coefficients h_k are calculated, the implementation of the filter is very straightforward.

As mentioned before, the transfer function of the FIR filter is of the form

$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n}$$

or, on the $j\omega$ axis:

$$H(e^{j\omega}) = \sum_{n=0}^{N-1} h_n z^{-j\omega n}$$

where $h(n)$ is the impulse response of the filter.

Figure 2.17 shows the block diagram of such a filter, in which the filter coefficients

are the impulse response coefficients. To implement such a filter an N^{th} order delay line, N multipliers and an N input adder are necessary.

2.4.3 Comparing the FIR and IIR structures

IIR filters have the advantage that a variety of filters can be designed using closed-form design formulas. IIR filters generally yield lower orders than those required for an FIR filter for the same specifications.

The FIR filter, on the other hand, is unconditionally stable, so it will not become unstable due to coefficient inaccuracies or variations. This makes the FIR filter especially suitable for adaptive applications, where coefficients are constantly varying. Also, the FIR filter can be made to possess an exact linear phase in a simple manner.

2.5 Existing SC FIR filter designs

There is a very wide variety of research done on SC filters. This section describes some of the related papers which describe line equalizers, echo cancellers [16, 17, 18], the fixed coefficient SC FIR filters [19].

2.5.1 Equalizers and echo-cancellers

Most of the literature on programmable SC filters describe application oriented designs, specifically line equalizers and echo-cancellers. They are very similar to

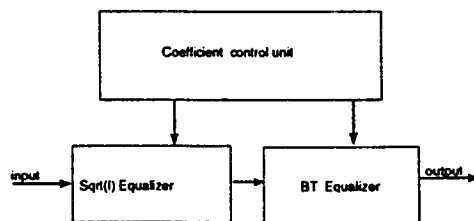


Figure 2.6: Programmable SC filter architecture

each other in that they share the same basic architecture shown in Figure 2.6. The f -equalizers and the bridged-tap (BT) equalizers (FIR), are the programmable filters, and the control unit contains the adaptive algorithm.

The line equalizers are designed to filter and recover digital data, and this greatly simplifies the FIR filter configuration. The recovered data is restricted to -1.0 , and 1 , so the information that is used in BT equalizers' multipliers is also restricted to -1.0 , and 1 . We can see this in the diagram of the CMOS line equalizer [18] shown in Figure 2.7, where the tap coefficient circuit and the summing circuit need to multiply an analog value to zeros or ones. This restriction simplifies the circuit design. In this example, the entire multiplying/summing circuit is implemented using one op amp. The clocking sequence defines whether the multiplication by a ± 1 or a 0 is realized.

2.5.2 SC FIR Filters

Sampled analog FIR filters are built using unit delay elements. However, these usually suffer from the fact that the number of operational amplifiers used for the

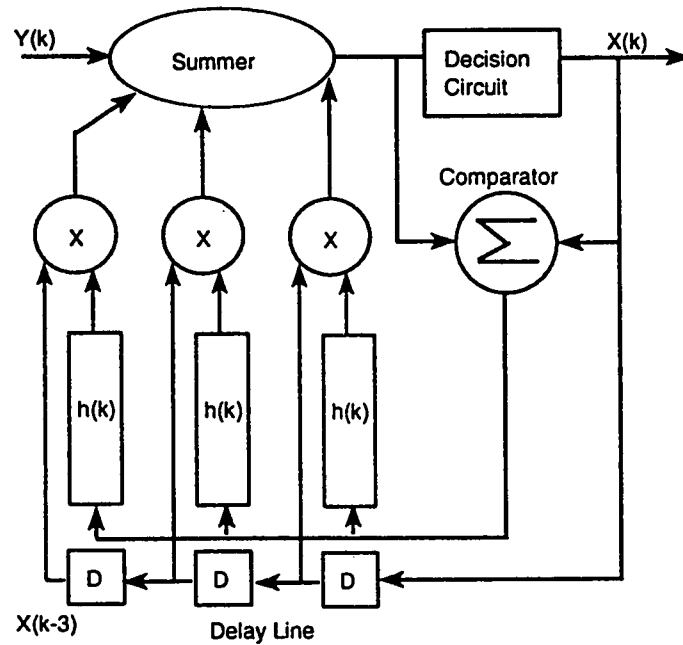


Figure 2.7: Block Diagram of BT equalizer

analog delay line is of the order of the length of the filter. Hence large chip area has to be used for relatively high order filters. A solution to this problem is the use of a multi-phase clocking scheme as employed in [20] to implement a delay line using a single op amp. This reduces the number of op amps in the FIR implementation; however the phasing circuitry becomes more complex as the order of the filter increases. A 10^{th} order filter section would exhibit too large a capacitor coefficient spread to be feasible for SC implementation. The LDI ladder structure can also be used to implement tapped delay lines by simulating the state variables of a uniform transmission line as shown in [11], where a 10^{th} order linear phase FIR low-pass SC filter was implemented.

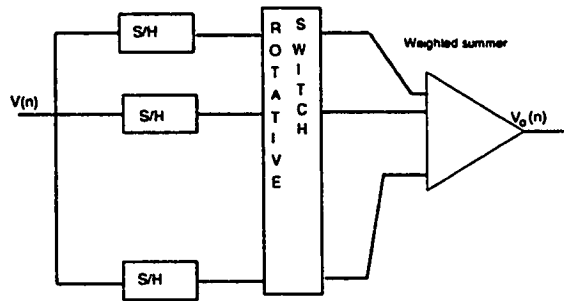


Figure 2.8: Block Diagram of FIR Filter

The adaptive finite impulse response filter based on the least-mean-square algorithm is also among the more commonly used adaptive filters. In most of these filters the realization is all digital. The realization of general adaptive FIR filters based on the LMS algorithm is described in [21]. However, this realization is advantageous in applications where the errors of the algorithm is larger than the error caused by the circuit non-idealities [21].

An SC realization of multiple FIR filters was described in [19]. In this example eight fixed-coefficient 32^{nd} order SC FIR filters were realized. The architecture used is based on the block diagram shown in Figure 2.4. The delay line was implemented using parallel sample and hold circuits with a rotative-switch and the multipliers and summers were realized using a single multiplying/summing configuration (weighted summer). The block diagram of this system is shown in Figure 2.8.

It becomes clear that to apply this circuit in the programmable case, some major changes have to be made. Firstly, extra circuits are necessary so the positive and negative coefficients can be programmed. Secondly, the feedback capacitor C_2 needs

to be programmable and an extra algorithm is necessary to calculate its value. Thirdly, this is not a stray-insensitive circuit, and finally, the quantization of C_2 introduces an extra noise into the system. Therefore, such a configuration cannot be used for programmable applications.

2.6 The Programmable SC FIR Filter

An architecture for a single chip programmable FIR filter was presented in [22]. This architecture is shown in Figure 2.9. It is a direct implementation of the digital FIR filter structure. It consists of a sample-and-hold block, an $N * N$ barrel switch, N programmable multipliers, and an N input adder.

The sample-and-hold block together with the barrel switch are equivalent to the analog delay line of the FIR filter. The sample-and-hold block consists of N sample-and-hold circuits in parallel. The input signal is sequentially sampled with an N -phased clock which has a frequency equal to $1/N$ of the sampling frequency. The barrel switch or the rotative switch, shifts the outputs of the sample-and-hold circuits so that at the output we have delayed versions of the input signal. The output of the delay line is fed into N independently programmable multipliers, where each multiplier is controlled by its corresponding filter coefficient, and it multiplies the analog voltage at its input by that coefficient. Each coefficient is defined by a binary number in sign-magnitude form. The adder, depending on the sign bit of

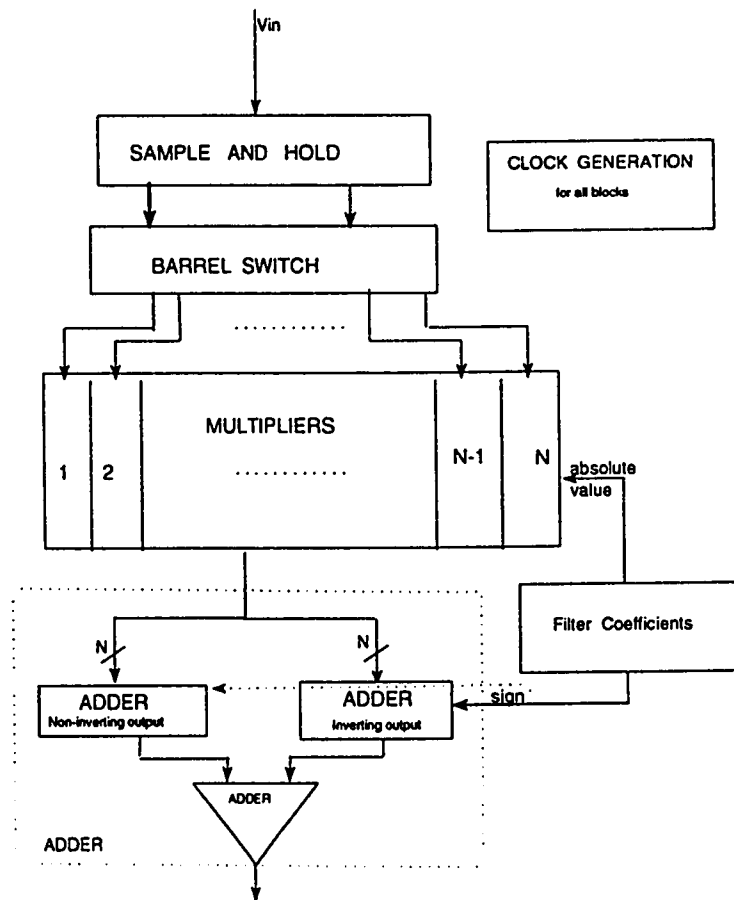


Figure 2.9: Block Diagram of a Programmable SC FIR Filter

the corresponding coefficients, adds or subtracts the outputs of the multiplier. An N input non-inverting adder sums the positive coefficients and N input inverting adder sums the negative coefficients. a two input adder is required to sum the end result.

2.6.1 Thesis Objective

It is clear that the architecture used in [22] has several advantages. Firstly, it has programmable coefficients, secondly, it uses a transversal structure, which enables direct implementation of existing adaptive algorithms. Finally, in contrast to some other designs, it is able to process any continuous analog signal. In [22] this architecture was used to implement a fourth order FIR filter. However the versatility of the architecture can be better studied for higher order filter performance, where all the minor problems get magnified. Our aim is to study the feasibility of achieving a higher order filter using this architecture. We wish to modify some of the basic building blocks in order to obtain an improved performance. An attempt will be made to obtain a 16^{th} order FIR filter based on this architecture.

The Integrated Circuit implementation of all the basic building blocks will be done using MAGIC version-6.3. CaZM simulation results will be provided wherever necessary.

Chapter 3

Design Considerations in MOS

Integrated Circuits

In this chapter the integrated circuit design of the SC filter components will be discussed. The operational amplifiers, switches and capacitors constitute the basic building blocks of the SC filter. The performance of any SC circuit will depend therefore on the performance and characteristics of these basic blocks and on the architecture used. The following section discusses these blocks, their IC design and presents some of the simulation results of the building blocks used in the SC circuits.

3.1 The Operational Amplifier

The most important building block in the design of switched-capacitor filters is the CMOS operational amplifier or the op amp. This section describes the op amp design procedures, designs an op amp for the SC FIR filter, and demonstrates the layout diagram and the simulation results of the op amp performance.

The two-stage CMOS op amp architecture was chosen for the programmable SC FIR filter. Figure 3.1 shows the general structure of the two stage op amp. The input differential stage is designed to provide high input impedance, low offset voltage and a high gain. The second stage is designed to perform additional gain and differential to single-ended conversion. The output buffer stage is needed in cases where the op amps are required to drive large capacitive loads on the chip. The circuit diagram of this op amp is given in Figure 3.2.

With reference to the circuit given in Figure 3.2 we now illustrate the design procedure for the op amp [1]. The design procedure begins by choosing a device length to be used throughout the circuit. This value determines the value of the channel length modulation parameter λ . The next step is to establish a minimum value of the compensating capacitor C_c . To obtain a 60° phase margin, the minimum value of C_c should be

$$C_c > 0.22 \times C_l$$

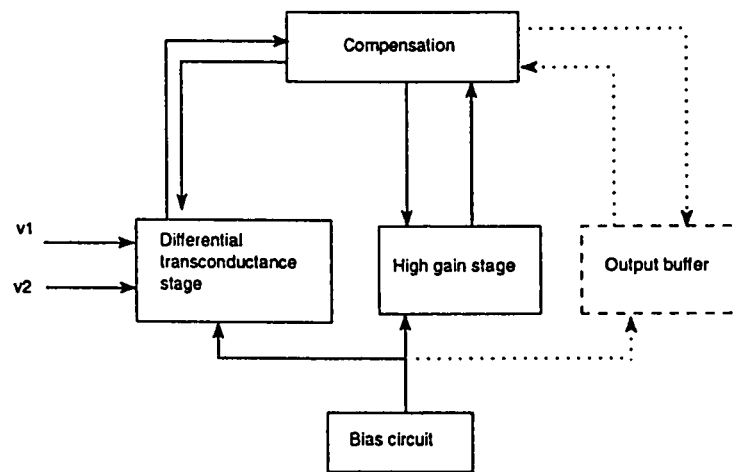


Figure 3.1: General Structure of a two stage Op Amp

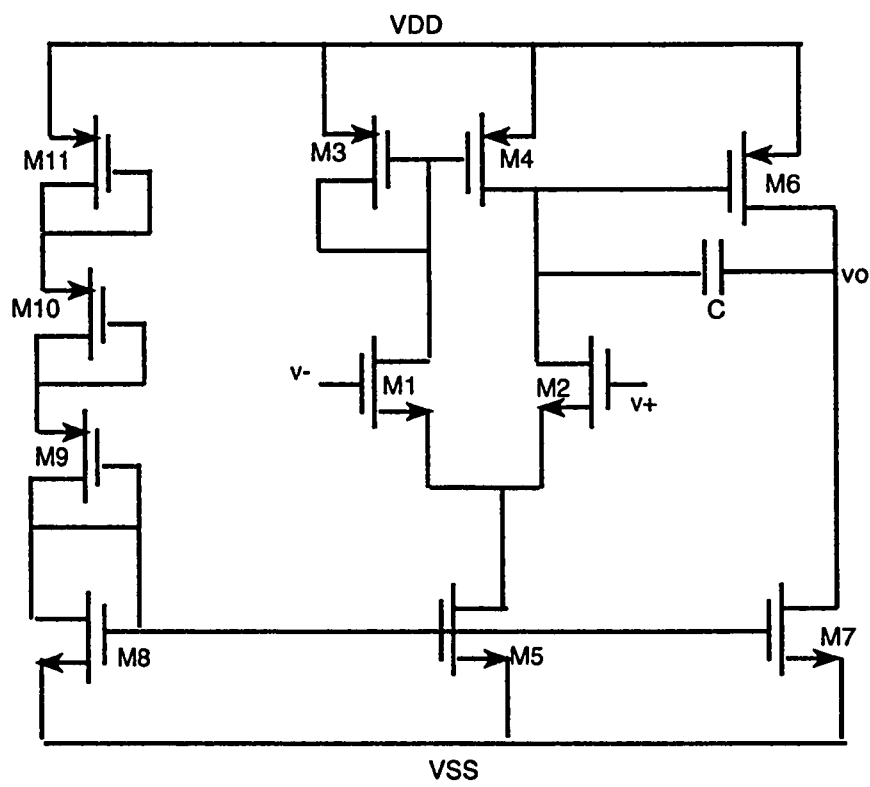


Figure 3.2: The two-stage CMOS op amp

Then the minimum value of tail current I_5 is determined to be

$$I_5 = SR(C_c)$$

The transconductance of the input transistors can be determined from C_c and GB as

$$g_{m2} = GB(C_c)$$

The aspect ratio of $M2$ is directly obtainable from g_{m2} as shown below.

$$S_2 = (W/L)_2 = \frac{g_{m2}^2}{K_2' I_5}$$

Then the saturation voltage of the transistor $M5$ can be calculated using the relation

$$V_{DS(sat)} = V_{in}(min) - V_{SS} - \frac{I_5^{1/2}}{\beta_1} - V_{T1}(max)$$

If the value of V_{DS5} is less than $100mV$ then the possibility of rather large $(W/L)_5$ may result. This has to be checked during the design. The transconductance g_{m6} can be determined using the relationship

$$g_{m6} = 2.2(g_{m2})(C_1/C_c)$$

The value of $(W/L)_6$ can be determined . From this value the current I_6 can be calculated by

$$\frac{g_{m6}^2}{2K_6' S_6}$$

I_6 is recalculated again using the balance equation

$$I_6 = \frac{(W/L)_6}{(W/L)_3} \times I_1$$

and the larger value is chosen. The device size of M_7 can be determined using the equation

$$S_7 = S_5 \left(\frac{I_6}{I_5} \right)$$

Now the gain can be checked against the specifications

$$A_v = \frac{2(gm_2)(gm_6)}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

Following the design procedures described above we proceed to design the op amp.

The design steps are as follows:

1. Choose the smallest channel length that will keep the channel length modulation parameters constant and give good matching for current mirrors.
2. Calculate the minimum compensating capacitor C_c according to the inequality $C_c > 0.22C_L$ and the lower limit gives 60 deg phase margin.
3. Find the minimum value of I_5 from the largest of the two values.

$$I_5 = [(SR)C_c]$$

$$I_5 = 10 \left(\frac{V_{DD} + |V_{SS}|}{2T_s} \right)$$

4. For the differential input stage, we first find $(W/L)_3$ from the specification on the maximum input voltage according to the relation

$$(W/L)_3 = \frac{I_5}{K_3[V_{DD} - V_{i(max)} - [V_{to3} + V_{T1min}]^2]} \geq 1$$

where the lower limit is required to reduce the gate capacitance keeping the effect of phase margin to a minimum.

5. Find $(W/L)_2$ to meet the required value of the unity gain bandwidth f_t

$$g_{m2} = \omega_t C_c$$

so that we get

$$(W/L)_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

6. Design for $M5$, find $(W/L)_5$ from the specifications on the minimum input voltage V_{imin} , in the following two steps

(a) The saturation voltage of $M5$ is

$$V_{DS5(sat)} = V_{imin} - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{t1(max)} \geq 100mV$$

(b) The aspect ratio of $M5$ is calculated as

$$(W/L)_5 = \frac{2I_5}{K'_5 [V_{DS5(sat)}]^2}$$

7. Find $(W/L)_6$ by choosing the second pole $p_2 = 2.2\omega_t$

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

so that

$$(W/L)_6 = \frac{g_{m6}}{K'_6 V_{DS6(sat)}}$$

and assuming

$$V_{DS5} = V_{DS6(min)} = V_{DS6(sat)}$$

we get

$$(W/L)_6 = \frac{g_{m6}}{K'_6 V_{DS6(sat)}}$$

$$g_{m6} = 2.2g_{m2} \left(\frac{C_l}{C_c} \right)$$

8. Find I_6 according to the relation

$$I_6 = \max \left[\frac{g_{m6}^2}{2K'_6 (W/L)_6} \cdot \frac{(W/L)_1}{(W/L)_3} I_1 \right]$$

9. Find $(W/L)_7$ to achieve the required current ratios,

$$(W/L)_7 = (W/L)_5 \frac{I_6}{I_5}$$

10. Check the gain and power dissipation from

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then increase $(W/L)_2$ or $(W/L)_6$. Alternatively I_5 or I_6 may be decreased.

12. If the power dissipation is too high then the only solution is to reduce I_5 and I_6 . However, this may require a corresponding increase in some of the (W/L) ratios for satisfying the input and output swings.

3.1.1 The Op Amp IC design

The design specifications for the operational amplifier with use in SC filters were obtained by using those of a general purpose op amp tailored towards the specific needs of our SC filter. We need a high gain op amp with the capability of driving a $25pf$ load. We shall use a buffer stage if required. For the initial design, the following specifications were chosen:

- Gain $A_v > 6000$
- $GB = 2MHz$
- $SR > 2v/\mu s$
- Common mode range $CMR > \pm 3.5V$
- $C_L = 25pF$
- Supply voltage = $\pm 5v$
- $V_{out} = \pm 4V$
- $P_{diss} < 10mW$

The process parameters taken from the CaZM file are (see Appendix) :

$$K'_n = 51\mu\text{amps/volt}^2$$

$$K'_p = 24\mu\text{amps/volt}^2$$

$$\lambda_n = 0.01/volt$$

and

$$\lambda_p = 0.02/volt$$

Referring to the op amp shown, and following the design procedures described above, we obtain the following results for each step.

1. Channel length= $10\mu m$
2. $C_C = 0.22C_L = 5.5pF$ which was later increased to $6pF$
3. $I_3 = SR \times C_c = 12\mu A$
4. $(W/L)_3 = 0.2$ and this is increased to one to minimize the gate capacitance
5. $g_{m2} = 2 \times 3.14 \times 6\mu = 37.6\mu S$ so that $(W/L)_2 = \frac{37.6^2}{51 \times 10^{-6} \times 12} = 2.3$
6. $V_{DS5(sat)} = 560mV \Rightarrow (W/L)_5 = 1.5$
7. The transconductance g_{m6} and the aspect ratio of M_6 is given by

$$g_{m6} = 2.2 \times 37.6 \times 25/6\mu = 345\mu S$$

$$(W/L)_6 = 14.4$$

8.

$$I_6 = \frac{345^2}{2 \times 24\mu \times 14.4} = 172\mu A$$

Also $I_6 = 14.4 \times 6 = 87\mu A$ We choose the larger value as $172\mu S$

9. $(W/L)_7 = 21$

10. We now calculate the gain of the op amp as

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$A_v = 14,000$$

11. The power dissipation is

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|) = 1.8mW$$

The currents I_5 , I_8 and I_{ref} are matched. so the transistors $M8, M5$ are matched. Their aspect ratios are equal. We assume $M9, M10, M11$ to be identical. They should satisfy the relation

$$V_{dd} + V_{ss} = V_{DS8} + V_{DS9} + V_{DS10} + V_{DS11} = 10$$

$$(W/L)_9 = (W/L)_{10} = (W/L)_{11} = \frac{2I_5}{K_n'[(V_{DS})_{sat}]^2}$$

This gives aspect ratios as $(W/L)_9 = (W/L)_{10} = (W/L)_{11} = 1.0$

Various simulations and some adjustments of the aspect ratios were necessary to obtain satisfactory performance of the op amp. The resulting final aspect ratios are

- $(W/L)_1 = (W/L)_2 = \frac{25}{10}$

- $(W/L)_3 = (W/L)_4 = \frac{8}{10}$

- $(W/L)_5 = \frac{20}{10}$

- $(W/L)_6 = \frac{140}{10}$
- $(W/L)_7 = \frac{210}{10}$
- $(W/L)_8 = \frac{20}{10}$
- $(W/L)_9 = \frac{10}{10}$
- $(W/L)_{10} = \frac{10}{10}$
- $(W/L)_{11} = \frac{10}{10}$

Figure 3.3 shows the layout of the op amp designed. The dimensions of the op amp are $286\mu m \times 315\mu m$. The slew rate is $5V/\mu s$, a settling time of less than $1\mu s$, and an openloop gain of about 9900.

Figure 3.4 shows the simulation results of the slew rate of the op amp. A unit pulse was applied to the input and the slope of the output was measured. The settling time shown in Figure 3.6 was also measured with the op amp in the unity gain configuration. Figure 3.5 shows the openloop gain of the op amp. Here the magnitude of the ac input voltage is $10mV$.

3.2 Switches

Figure 3.7 shows the simplest MOSFET switch and its equivalent circuit including the associated parasitics. This switch has a larger clock feedthrough and a small

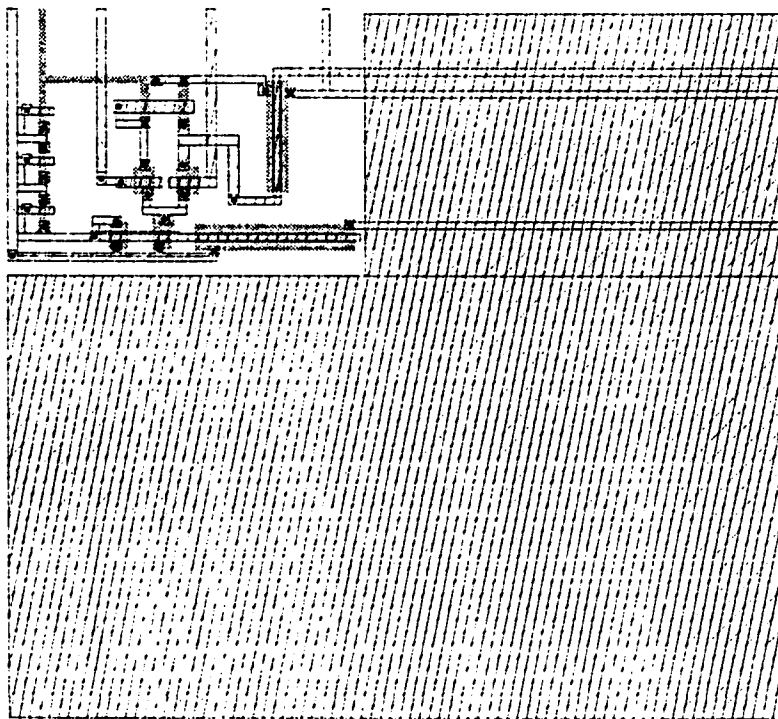


Figure 3.3: IC layout of the Op Amp ($area = 286 \times 315 \mu m^2$)

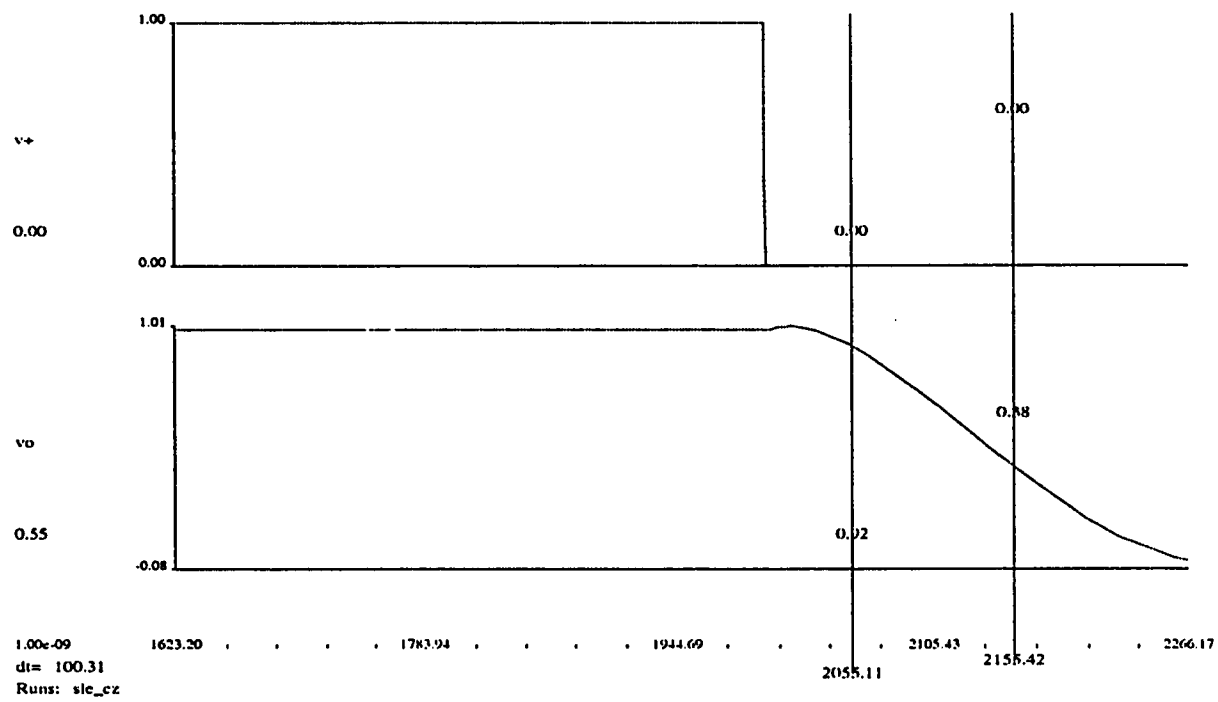


Figure 3.4: Slew rate

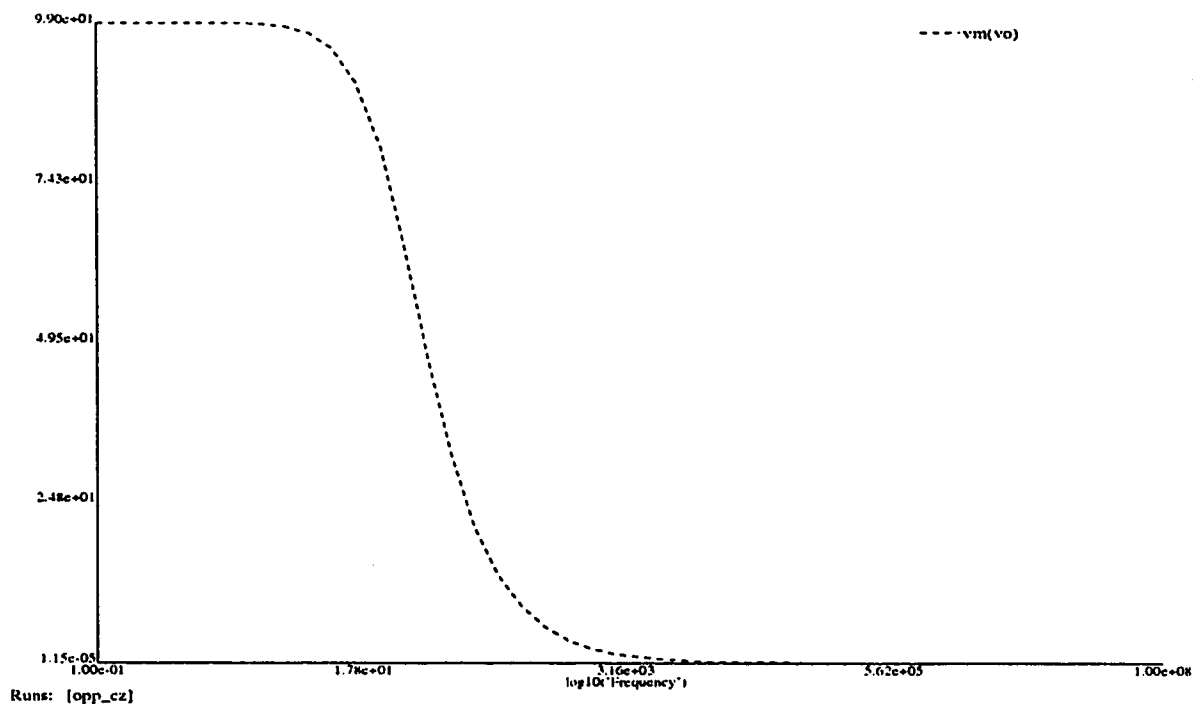


Figure 3.5: Op amp gain simulation

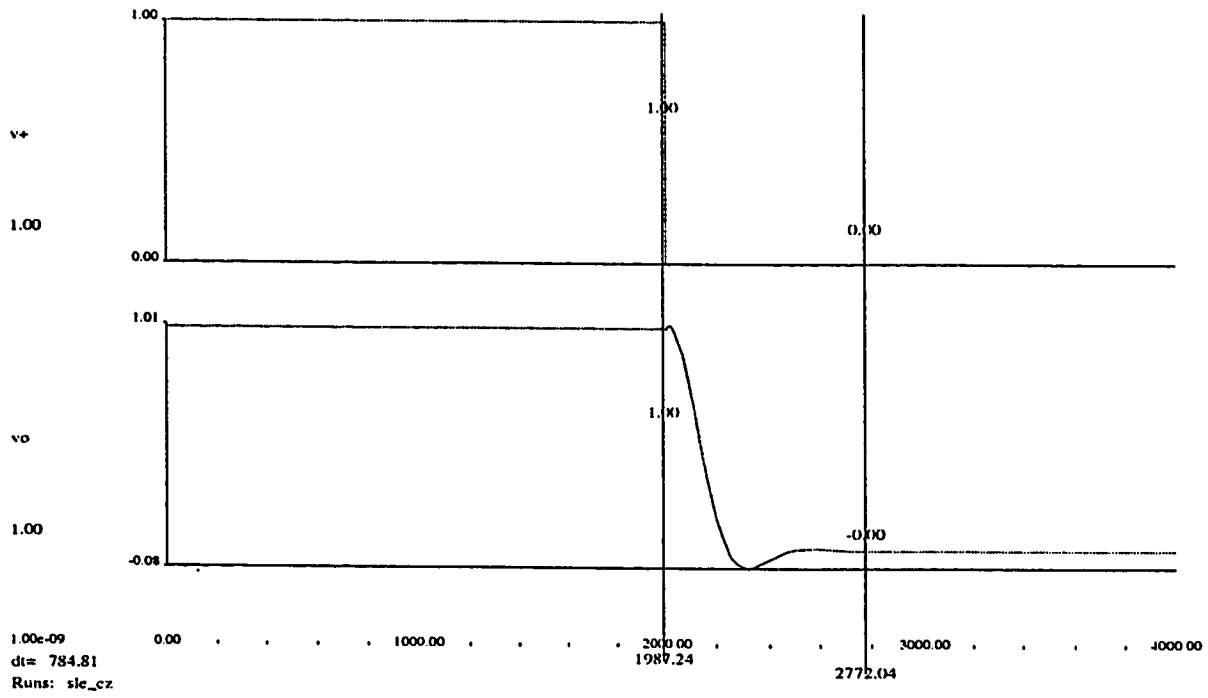


Figure 3.6: Op amp settling time simulation

voltage range for the signal by comparison with the CMOS switch. Also for NMOS and PMOS switches the resistance varies greatly as a function of signal voltage. The NMOS switch has its resistance increased by an order of magnitude for input voltages close to power supply voltage. This reduces greatly the signal voltage range in comparison to the CMOS switch shown in Figure 3.8. The CMOS switch has a fairly constant ON resistance because, as one of its transistors enters the cutoff region the other one is conducting fully.

Another important advantage of the CMOS switch is that the clock feedthrough is reduced due to the complementary clock signals used in this configuration. However in the practical case the switch injects an amount of charge into the holding capacitor (due to the parasitic capacitances), therefore causing the output voltage to be slightly different from the input.

3.3 Capacitors and Capacitor arrays

In this section the construction of capacitors and capacitor arrays will be described. There are many capacitor configurations possible in CMOS technology, the most common being the polysilicon-diffusion and the poly-silicon-poly-silicon.

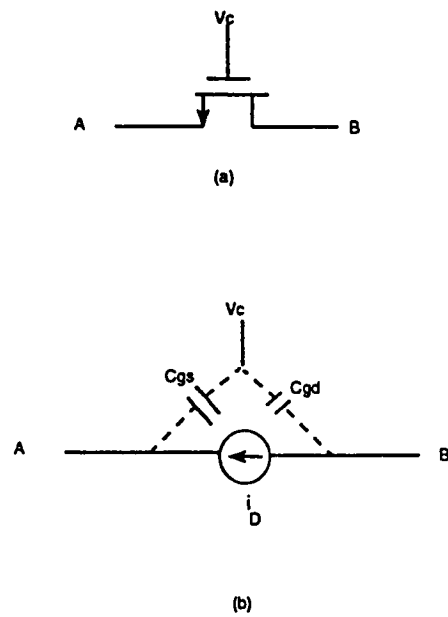


Figure 3.7: a)The MOS switch b) Model with parasitics

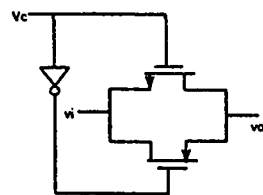


Figure 3.8: The CMOS switch

3.3.1 Parasitic Capacitances

Parasitic capacitances are inherent in all the MOS capacitor structures. These are unwanted capacitors and should always be taken into account when IC capacitors are used. The typical capacitor is constructed of a bottom and top plate as shown in Figure 3.9(a) and the capacitance is given by,

$$C = A\epsilon_{ox}/t_{ox} = C_{ox}A$$

where A is the area of a plate and ϵ_{ox} is the dielectric constant and t_{ox} is the oxide thickness. There is a capacitance between the top plate and the ground and the bottom plate and the ground. These parasitic capacitances can be of the order of the desired capacitance itself and should always be taken into account in IC design. The *bottom plate* parasitic capacitance is much larger than the top plate, so in many cases this plate is connected to a low impedance node.

To increase the capacitance density, a *multiple-layered capacitor* [22] can be used as shown in Figure 3.9(b). In this case we can increase the capacitance density by a factor of 1.5 or more, depending on the oxide thickness, *without* a significant change in the parasitic capacitances. In this case, $C = C_{ox}'A$ where

$$C_{ox}' = \epsilon_{ox}/t_{ox}' = \epsilon_{ox} \frac{(t_{1ox} + t_{2ox})}{(t_{1ox}t_{2ox})}$$

t_{1ox} and t_{2ox} are the oxide thickness of the upper and lower capacitors respectively.

If $t_{1ox} = t_{2ox} = t_{ox}$, then $C = 2C_{ox}A$ [22].

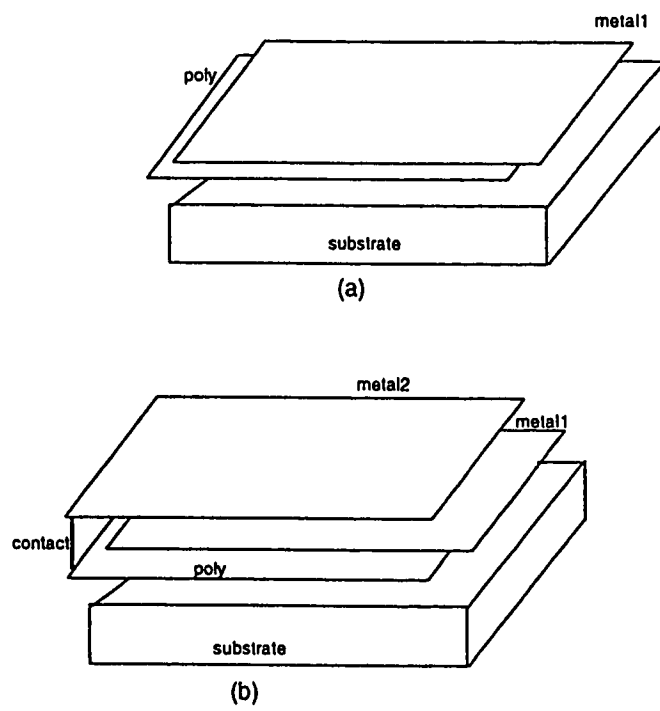


Figure 3.9: (a) Common capacitor (b) Multiple-layered capacitor

3.3.2 Capacitor-ratio errors

The performance of switched capacitor filters is determined by the capacitor ratios, therefore the errors involved in these ratios constitute an important design consideration. The sources of these errors are now discussed briefly:

1. Random Edge Variations

Figure 3.10 shows the top view of a MOS capacitor, in which the edges of the electrodes exhibit random edge variations. The nominal capacitance value is $C = \frac{\epsilon A}{l}$ and due to the random edge variations in the area we have

$$\Delta C = \frac{\epsilon}{l} [(W + \Delta W)(L + \Delta L) - WL]$$

so that

$$\frac{\Delta C}{C} = \frac{\Delta W}{W} + \frac{\Delta L}{L}$$

It can be shown that the standard deviation of ΔC will be minimum if $W = L$, which means that *the capacitor shape should be square* [5].

2. Under-cut Error

This results from the uncontrollable lateral etching of the plates of the capacitor along its perimeter in the fabrication process as shown in Figure 3.11. This gives rise to a decrease in value of capacitance proportional to the perimeter.

With the capacitor ratio

$$\alpha = \frac{C_1}{C_2} = \frac{W_1 L_1}{W_2 L_2},$$

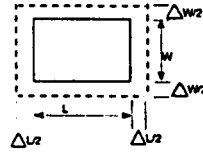


Figure 3.10: Random Edge Variations in MOS capacitor

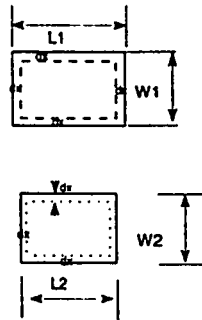


Figure 3.11: Undercut Error

the undercut error results in the actual ratio being equal to

$$\alpha_1 = \frac{W_1 L_1 - 2(W_1 + L_1)\Delta x}{W_2 L_2 - 2(W_2 + L_2)\Delta x}$$

where Δx is the depth of the undercut. The undercut error can be avoided if $W_1 = L_1$ and $W_2 = L_2$. A very common technique to avoid the undercut error is to connect *identical unit capacitors* to construct larger ones.

The geometry that minimizes these errors is the *square* capacitor, because the ratio of the perimeter to the area is the smallest. Another technique used to maximize the matching of capacitors is by choosing an appropriate unit capacitor (C_u), and constructing all other capacitors by the parallel connection of these unit capacitors. Finally, it is important to keep matched capacitors as close as possible to each other

to minimize the oxide effects.

Keeping these simple facts in mind we shall construct capacitor arrays in our design. A unit capacitor C_u of $0.5\mu F$ was chosen. These unit capacitors will later on be connected together to form other values of capacitances that compose the programmable capacitor arrays (PCA's).

The binary weighted PCA is the most efficient configuration and is shown in Figure 3.12. X and v_G are the programmable capacitors terminations, and D_1 to D_N constitute the digital control word. This structure ensures programming of capacitor values using simple digital inputs. In this case a binary byte would control the switches which connect each capacitor either to programmable capacitors terminal v_G or to ground. The sum of the capacitances of the capacitors connected to v_G gives the total capacitance between X and v_G as ,

$$C = \sum_{i=1}^N D_i 2^{i-1} C_u$$

As was mentioned earlier, parasitic capacitors are unavoidable in IC design. However there are several techniques that minimize the effects of these parasitic capacitors. The top plate of each capacitor has a smaller parasitic capacitance. This plate is connected to X and the bottom plate to v_G so that the latter terminal is loaded with the capacitance. In practice it is important to make the proper connections in order to minimize the effects of parasitic capacitances at v_G . Usually

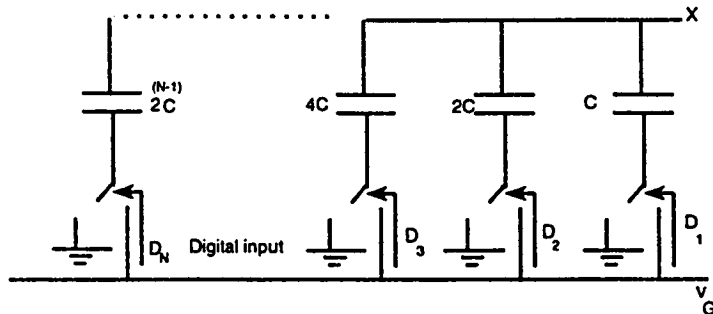


Figure 3.12: PCA structure

this terminal is connected either to the *physical ground* or to *virtual ground* of the op amp.

3.4 Conclusion

In this chapter, we described the op amp design procedure, designed an op amp for the SC filter and demonstrated some of the simulation results. It was found that the op amp had an openloop gain of 9900, a slew rate of $5v/\mu s$ and a settling time of less than $1\mu s$. These results are within the required specifications. We also discussed certain capacitor configurations and showed that the binary weighted PCA structure is the most ideal for programmable applications. The importance of *stray-insensitive design* was emphasized. The basic blocks discussed in this chapter, ie. op amps switches and capacitors will be used in our design to construct the programmable SC FIR filter.

Chapter 4

The Programmable SC FIR Filter

This chapter discusses the building blocks of the SC FIR filter. First the architecture of the digital FIR filter is presented. The various building blocks in the architecture are replaced by suitable SC circuits. The simulation results of each of these blocks are presented and analysed. Finally, the complete IC layouts of 8th and 16th order filters are given. The simulation results are presented and discussed.

4.1 The Digital FIR Filter Architecture

The architecture of a digital FIR filter is shown in Figure 4.1. It consists of an N^{th} order delay line, N multipliers and an N input adder. We wish to use this architecture to implement an SC filter. The many advantages of using the digital filter architecture are obvious. By a direct implementation of the digital architecture,

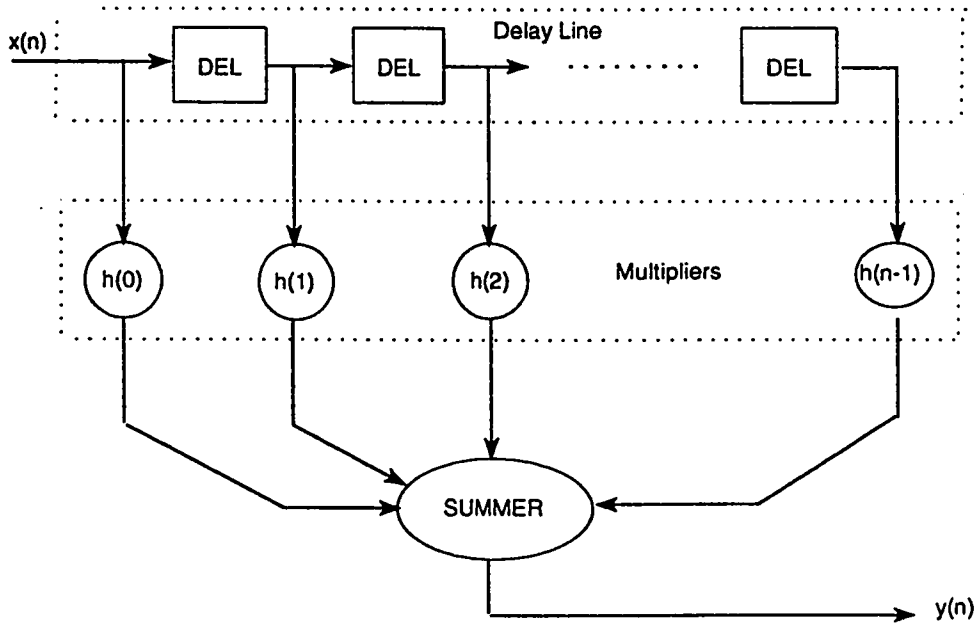


Figure 4.1: FIR Filter Block Diagram

one can process digital as well as analog signals. In addition to this, one can have the advantage of programming the coefficients. Moreover the same filter structure can be used to meet any desired filter specifications. Also, all the research done on the digital FIR filter and the algorithms that are already available can be directly applied to the SC filter. In other words, the SC filter has all the advantages of a DSP system with the added advantage of being able to process an analog signal.

With the architecture already available, the implementation is quite straightforward. One only needs to replace the various digital blocks by suitable switched-capacitor circuits with an emphasis on IC implementation. However, the practical considerations, or more precisely, the effects of stray-capacitances have to be taken

into account. Attention has therefore to be given to the use of building blocks which perform the same function as those of Figure 4.1 but are *insensitive* to parasitic capacitances.

4.2 The Switched-capacitor Delay Line

As mentioned earlier, the digital FIR filter consists of unit delays, multipliers and an adder. Each of these blocks can be replaced by switched-capacitor circuits. Thus the delay units of the digital FIR filter can be replaced by an analog delay line. Stray free analog delay circuits are very difficult to implement with a full cycle delay requiring at least one op amp [23]. Therefore an N^{th} order filter comprising of unit delay cells would require at least N op amps thus increasing the cost of a direct implementation.

A multi-phase clocking scheme was employed in [20] to reduce the number of op amps in the delay line. A fourth-order delay line employing this scheme is shown in Figure 4.2. The main feature of this delay line is that a single op amp is used. For an N stage delay, N feedback-capacitors (memory elements) and an equal number of clock phases are required. The signal transport in this delay line is realized by shifting the same charge from one stage to the next. A compact delay line can be constructed by connecting such delay cells in cascade. However, in order to achieve a complete charge transfer, the inverting node of the amplifier must be at virtual

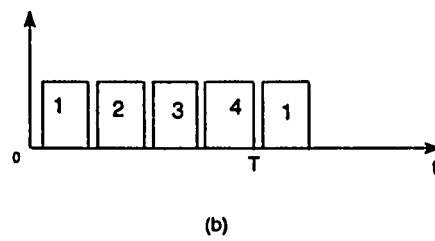
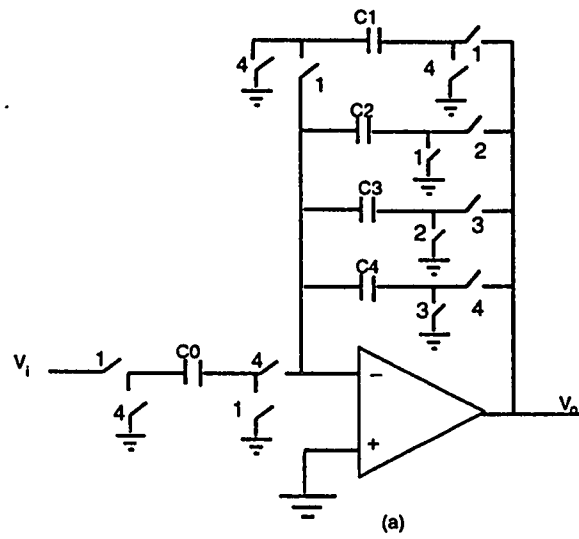


Figure 4.2: (a) 4 stage delay line (b) 4-phase non-overlapping clock.

ground. This generally requires a high-gain op amp. Also the time-multiplexing of the operational amplifiers imposes a stringent requirement on the settling time of the op amp. For example for a 16^{th} order filter, the operational amplifier would have to settle 16 times during a full clock cycle. In addition to this, the capacitor mismatch also causes an error in the system. All these drawbacks make it unfeasible for our filter application.

We next consider the delay line structure used in [22], which is shown in Figure 4.3. It consists of a sample and hold and a rotative switch. The sample-and-hold block consists of N sample-and-hold circuits in parallel. The input signal is sequentially sampled with an N -phase clock which has a frequency equal to $1/N$ of the sampling frequency. The input op amp shown in Figure 4.3 is shared by all the circuits in order to cancel the non-ideal effects of the buffers.

The rotative switch, shifts the outputs of the sample-and-hold circuits so that at the output, we have delayed versions of the input signal (v_i). $ph1$ to phN are N non-overlapping phases of the clock. The output z is always connected to the input signal v_i , at the clock phase $ph1$. $z(n-1)$ is connected to the most recent sample of the input signal and so on. For example, at $ph1$, $v(n)$ is connected to buffer 1 which is connected to v_{in} through the input op amp. $z(n-1)$ is connected to buffer N (through section N of the rotative switch), which is holding the latest sample of the input v_{in} . Finally $v(n-N)$ is connected to buffer 2 which is holding the oldest sample of the input.

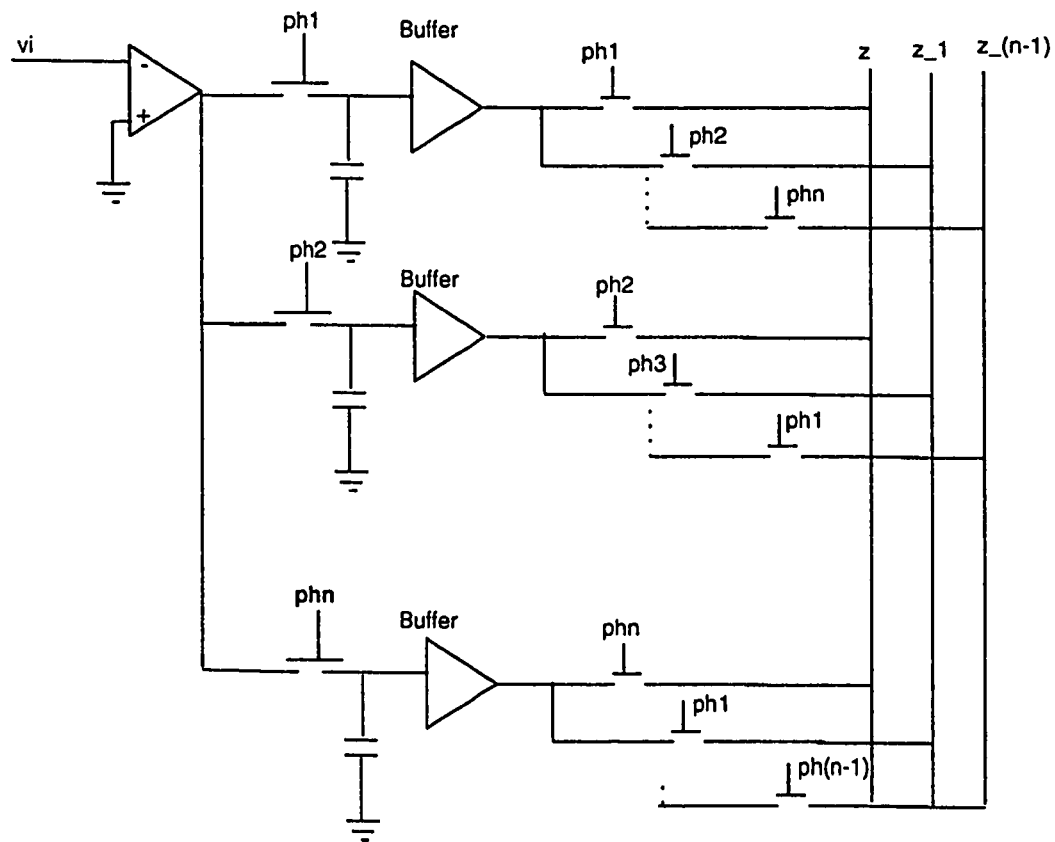


Figure 4.3: Delay line with SH and barrel switch

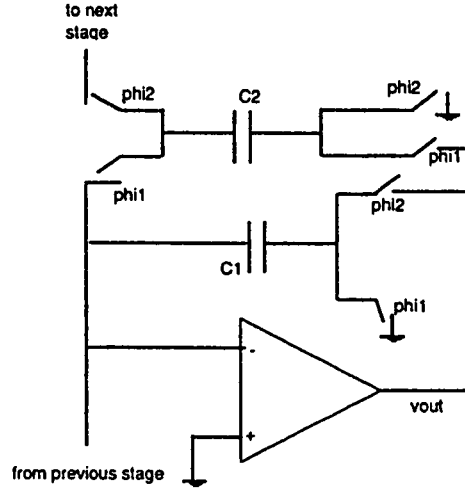


Figure 4.4: Single stage of the stray insensitive delay line

The architecture of this delay line has several drawbacks. Firstly, it needs N^2 switches to implement an N th order filter structure. Secondly, it needs an N phased clock for proper operation, and finally it requires a larger layout area. It is clear that extra timing signals are required apart from the two phased clock for proper functioning of the entire system. It may be advantageous for small delays but is unsuitable for higher delays due its cost of implementation.

The need for the extra timing signals can be eliminated by using the unit delay structure [23] shown in Figure 4.4.

The operation of this delay line is as follows. During the phase ϕ_2 , the capacitor C_1 is charged by the previous stage to a new output voltage, while C_2 transfers its charge to the subsequent stage. In the next phase ϕ_1 , the output voltage remains

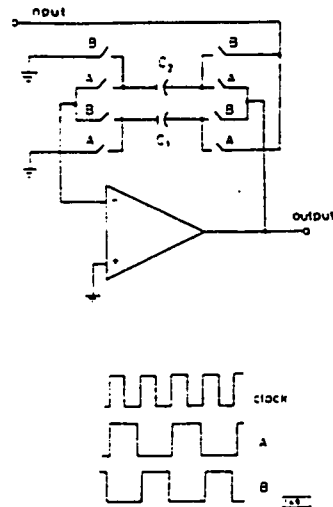


Figure 4.5: delay unit which is insensitive to capacitor mismatch and stray capacitances

constant. C_1 transfers its charge to C_2 , which had been discharged in the previous phase. The circuit is completely *stray insensitive* since none of the capacitors are switched between non-zero voltage driven nodes.

A full unit delay requires one op amp, two capacitors and six switches. It is advantageous in comparison to the delay line with the sample and hold and the barrel switch as it uses less number of switches. However, the capacitor mismatch will cause a gain error, but this mismatch will not cause an infinite impulse response.

The capacitor mismatch can also be eliminated [24] by using the circuit shown in Figure 4.5. It is driven by a two phase clock having a frequency equal to half the main clock frequency. At phase A, the capacitor C_1 samples the input, while C_2 is

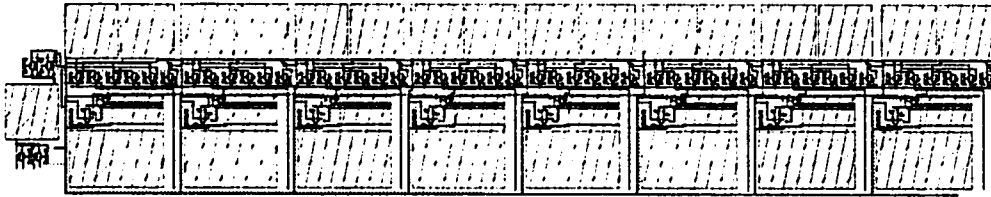


Figure 4.6: Layout of the eighth order delay line ($area = 620 \times 3255 \mu m^2$)

connected across the operational amplifier. Thus the output of the op amp is equal to the voltage across C_2 . At phase B, C_1 and C_2 are interchanged. Thus the output voltage assumes a new value. At the same time the present input is sampled by C_2 . The circuit functions as a delay line having a delay equal to one clock interval. The circuit is insensitive to stray capacitances and also to the capacitor mismatch as the operation of the circuit is independent of the ratio of C_1 and C_2 . However, its drawback lies in the fact that the two phased clock needs to run at half the main clock frequency.

In order to be able to drive the entire system by a single two-phased clock, we have used the circuit shown in Figure 4.4 as a unit delay. Figure 4.6 shows the

layout of the entire delay line. Unit capacitors of $2.0pF$ were used in the layout.

In Figure 4.7 the simulation results of the delay line are shown. The input of this block is v_i and the outputs, v_1, v_2, \dots, v_N , are connected to the multipliers. A pulse of $1V$ is applied to the input and the propagation of the input can be seen. The simulation results are very satisfactory and one can observe that 99% of the signal is available at every stage of the delay line. The slight deviation from the ideal, apart from the finite gain of the op amp, is due to the capacitor mismatch. Larger unit capacitors can be used to further enhance the performance of the system.

In this section, we studied some delay line configurations and discussed the advantages and disadvantages of each one. We found that while the delay line in [20] has a very compact structure, it requires a time multiplexing of op amps and a multiphased clock and is therefore unsuitable for the digital filter application. We next considered the delay line structure with the sample-and-hold and the barrel switch. It was shown that it requires N^2 switches N buffers and an N phased clock, and is therefore unsuitable for higher order filters because of the extra circuitry involved. The section also showed that the delay line described in [24] is insensitive both to the capacitor mismatch and stray capacitances. However it requires a two-phased clock running at half the main clock frequency. To be able to drive the entire system by a single two-phased clock, we used the delay line structure shown in Figure 4.4. From the simulation results, it was found that the delay line used had an excellent performance.

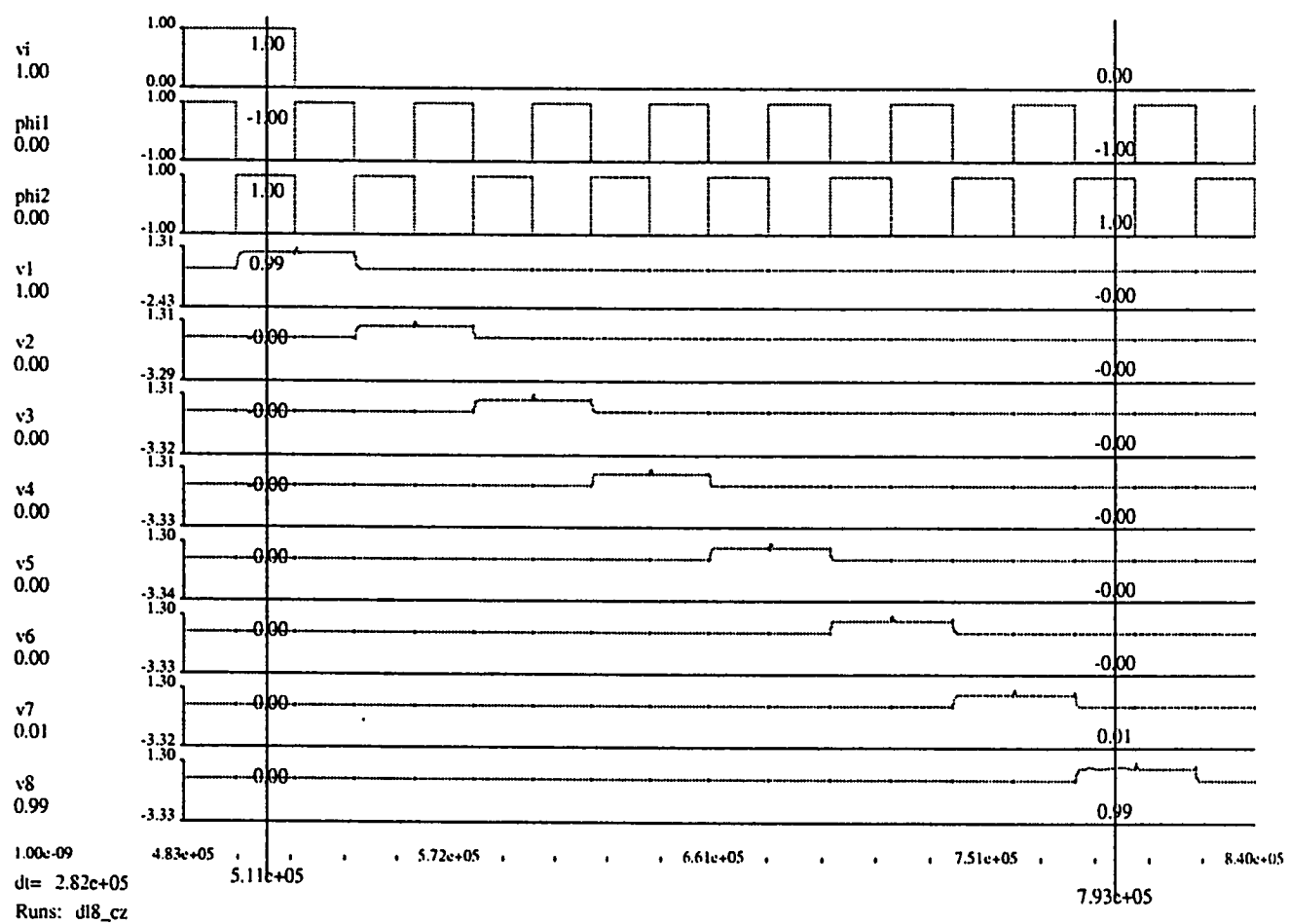


Figure 4.7: Simulation results of the delay line

4.3 The Multipliers

The *multiplier* is a circuit that multiplies the voltage at its input, by a digital number which is the filter coefficient. The output of the delay line is fed into N independently programmable multipliers. The circuit diagram of the multiplier is shown in Figure 4.8. The programmable capacitor array (PCA) described in the previous chapter is used to program the multiplier. We have used the sign-magnitude representation in our design. The value of the smallest capacitor was taken as $0.5pF$ in order to maintain a smaller layout area. Each multiplier is controlled by its corresponding filter coefficient, and multiplies the analog voltage at its input by that coefficient. Each coefficient is defined by a binary number with a “sign-bit” as the MSB and the absolute value of the coefficient for the remaining bits. The output of each multiplier is given as:

$$v_{out} = -C_i/C_f \times v(i); i = 1, \dots, N$$

The circuit diagram of the multiplier is given in Figure 4.8. At ϕ_{i1} , C_f is discharged. Also at ϕ_{i1} , the input capacitor C_1 is grounded on the one side by the switch and on the other it is connected to the virtual ground of the op amp. At ϕ_{i2} , the capacitor C_1 is connected to v_{in} and this will cause a charge of $Q = v_{in}C_1$ to flow into C_f . The output voltage change is $\Delta v_{out} = -Q/C_f$. Therefore, the output of the circuit is given by,

$$v_{out} = -\frac{C}{C_f} v_{in}$$

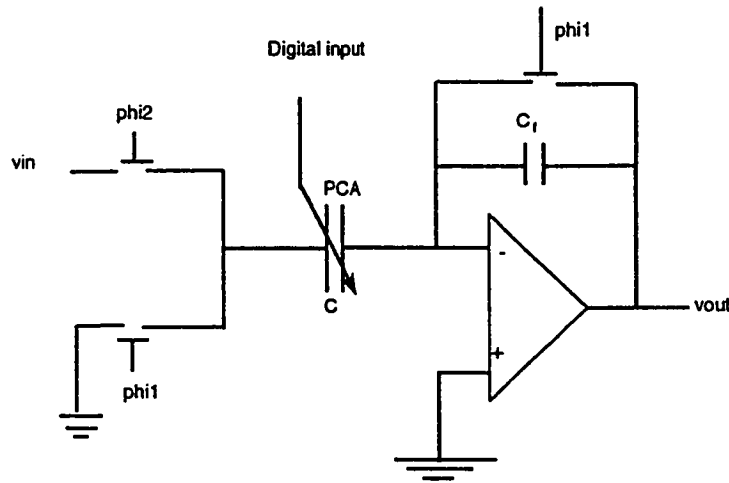


Figure 4.8: Circuit diagram of the multiplier

Since the bottom plate of the capacitor is switched between ground and virtual ground, the circuit is *insensitive* to parasitic capacitance.

We have used a PCA with 6 bits of resolution. The PCA structure is shown in Figure 4.9. Together with the sign bit a 7 bit coefficient resolution is obtained. The ratio C/C_f can vary from 0.0000 to 3.9375 with a step size of 0.0625. In order to have larger capacitance per unit area, we have used the *multi-layered* capacitor described in chapter 3. It is clear that the clock signals will have to be non overlapping or else the input signal will be momentarily grounded, and more importantly, the charge flowing through C will not flow entirely into C_f . Each filter coefficient is defined by a unique multiplier. The filter coefficients are first multiplied by the order of the

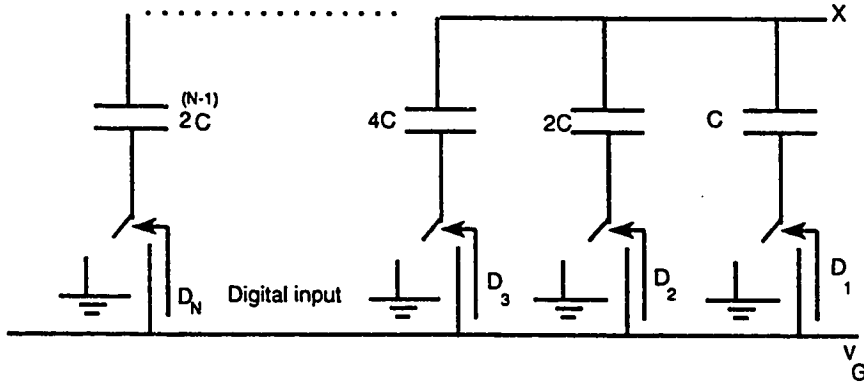


Figure 4.9: PCA structure

filter and are then programmed into the filter.

It was mentioned that the ratio C/C_f can vary between 0.0000 and 3.9375. However, care has to be taken to operate within the linear range of the op amp, otherwise the output might saturate.

The layout of the programmable multiplier is shown in Figure 4.10. We applied a constant 1V input to the circuit and observed the response by changing the tap coefficients. Figure 4.11 indicates the simulation results of the multiplier. These results are also shown in Table 4.1.

In this section we described the circuit diagram, the IC implementation and simulation results of the multipliers. We found that the multipliers had a satisfactory performance. We could have increased the number of quantization bits from 7 to 8 but found that the parasitic capacitance of the top plate also has an effect if the number of bits are increased thereby deteriorating the overall performance. We



Figure 4.10: Layout of the multiplier ($area = 363 \times 2310 \mu m^2$)

filter coefficient	ideal results	simulated results
00.0001	-0.063	-0.06
00.0010	-0.125	-0.12
00.0100	-0.25	-0.24
00.1000	-0.50	-0.51
01.0000	-1.00	-1.02
10.0000	-2.00	-2.00
10.1111	-2.9375	-2.96

Table 4.1: Simulation results of the multiplier

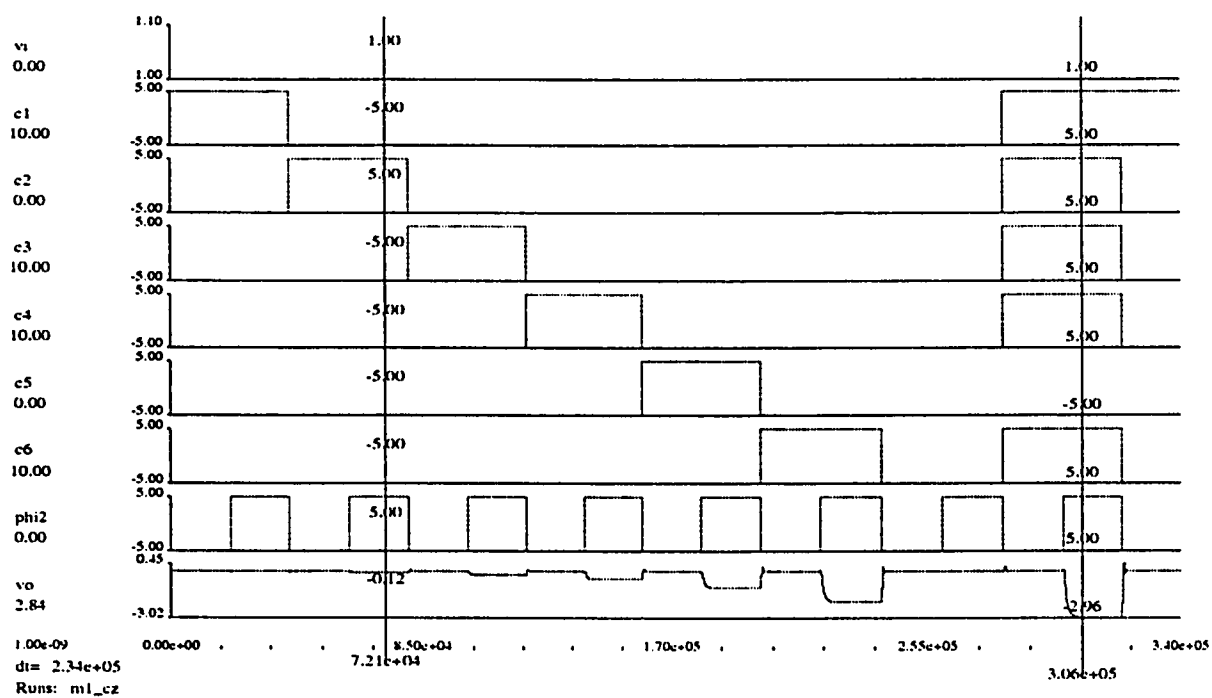


Figure 4.11: Simulation results of the multiplier

therefore restricted the PCA quantization to a maximum of seven bits.

4.4 The Adder Block

The adder block consists of three adders. An N input inverting adder to add the negative coefficients, an N input non-inverting adder to add the positive coefficients and a two input adder to sum the result. The circuit diagram of the inverting adder is shown in Figure 4.12. It is similar to that of the multiplier and is also *stray-insensitive*. However, in this case the capacitors at the input of the op amp are equal, thereby simplifying the layout. A non-inverting adder is obtained by adding a switched-capacitor inverting stage to the inverting adder. This ensures that the positive and negative coefficients are added at the same phase of the clock. However, it requires an extra op amp for the sign inversion. A two input adder is used to add the final result.

The inverting adder has the following output,

$$v_{out} = -\frac{1}{N} \sum_{i=1}^N v(i)$$

v_{out} is *only valid* at $\phi i2$. The adders sample the outputs of the multipliers at $\phi i2$.

The fraction $\frac{1}{N}$ is used to prevent the saturation of the adder op amp and also to ensure that the effect of capacitor mismatch is *minimized*. For the 8th order filter, the multiplying coefficient's maximum value is 3.9375, therefore the overall multiplying and adding circuits have an effective multiplying coefficient that varies

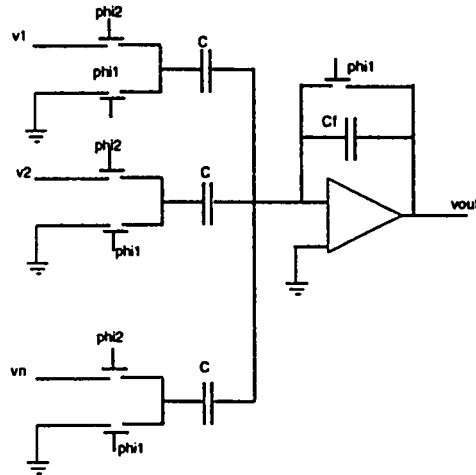


Figure 4.12: Circuit diagram of the inverting adder

v1 to v8	$\sum v(i)$	$vo = -\frac{1}{8} \sum v(i)$	simulation
0.1,0.2,0.3,0.4,0.5,0.6,0.7,0.8	3.6	-0.45	-0.45
0.5,0.5,0.5,0.5,0.5,0.5,0.5,0.5	4.0	-0.50	-0.51

Table 4.2: Simulation results of the inverting adder

between -0.49218 and $+0.49218$ with a 7 bit resolution that corresponds to a step size of 0.0078.

The layout of the adder is shown in Figure 4.13. Different combinations were tested for the adder circuit and the simulation results were observed. The simulation results are shown in Figure 4.14 and Table 4.2.

In this section, we described the adder structure. We could have used a single op amp to add and subtract the positive and negative coefficients. But such a circuit suffers from parasitic capacitances at its input. We therefore used the adder

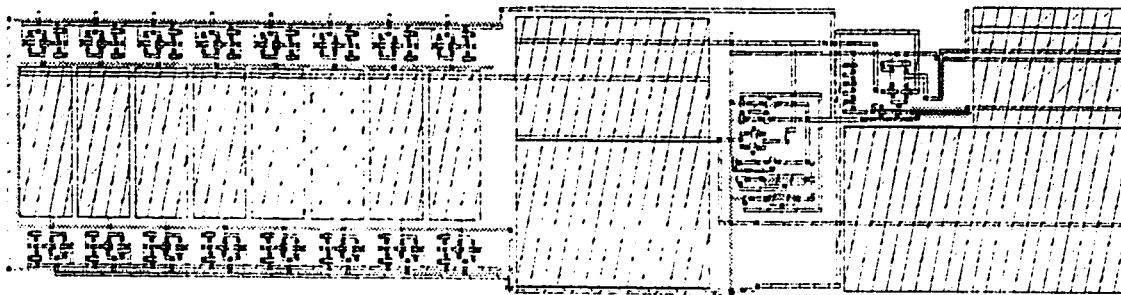


Figure 4.13: Layout of the inverting adder ($area = 312 \times 1240 \mu m^2$)

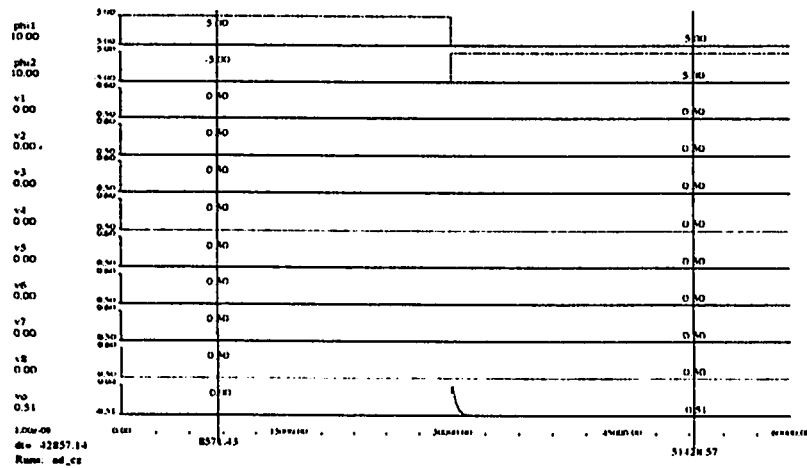
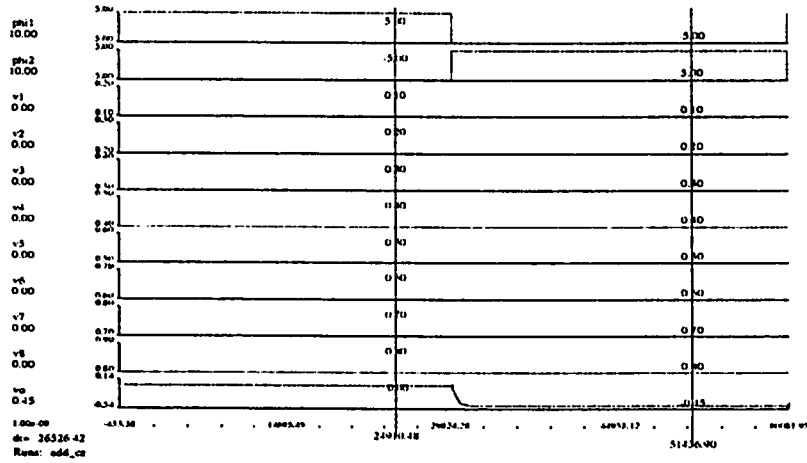


Figure 4.14: Simulation results of the eight input adder

structure shown in Figure 4.12. To be able to add and subtract at the same phase of the clock, we added an SC inverting stage to the inverting adder in order to obtain a non-inverting adder.

4.5 Limitations of the Building Blocks

The basic building blocks of any switched-capacitor circuit are the operational amplifier, the switch and the capacitor. The performance of any SC circuit depends mainly on the performance of these basic building blocks. In this section, we consider the limitations of the filter performance due to the limitations in these blocks.

It was mentioned in chapter 3 that the op amp had a gain of 9900. This finite gain of the op amp will result in an incomplete charge transfer. Also, the random offset voltage of the op amp will introduce an error at the output. However, this can be overcome using the auto-zeroing techniques [1].

Another limitation of the building blocks is the non-ideality of the switches. We have used the CMOS switch shown in chapter 3. The important parameters of the switch are the ON resistance and the OFF resistance. The effect of the ON resistance can become important during the charge transfer phase. For successful charge transfer, the time constant associated with the ON resistance of the switch $R_{on}C \ll T/2$ where T is the time period of the clock. The OFF resistance of the switch will result in a leakage current into the holding capacitor that can cause an

offset voltage at the output.

Another serious limitation of the switch is the clock-feedthrough. Although the CMOS switch can, in principle, cancel the clock feed-through, the cancellation is not perfect due to the following two reasons. One is that the feed-through capacitances of the n-channel device are not necessarily equal to the feed-through capacitances of the p-channel device. The second is that the turn-on delay is not the same for each type of transistor and so the channel conductances do not necessarily track each other during turn-on and turn-off.

All these factors contribute to limit the performance of the filter. Appendix A shows the model of the MOS transistor listing all the non-idealities considered by CaZM.

4.6 Comparison with the Previous Design

In this section, we compare our design with that of [22]. It was mentioned that the delay line used in [22] has several drawbacks. Firstly, as the number of switches increase by N^2 , it is not possible to construct a higher order delay by cascading two similar delays. Secondly, the clock feed-through caused by the switches can be a major source of error in the system. It was found in [22] that even a small 4th order delay line resulted in a clock-feedthrough of 30mV. This effect is practically unacceptable for higher order filters. Finally, the structure used is unsuitable for

VLSI implementation. We modified the delay line in the filter by using identical stray-insensitive delay units. This makes the structure highly suitable for VLSI implementation as only one mask of a unit delay is required to construct a delay line of any order. Also, the operational amplifier was designed to have a higher gain, a higher common mode range, and the ability to drive large capacitive loads. By these modifications, we were able to simplify the layout and to drive the entire filter by a single two-phased clock.

4.7 Suitability for VLSI implementation

An important goal for any designer is to make the architecture simple so that it could be easily implemented on a VLSI chip. This problem is not a very critical one for digital circuits as the OASIS silicon compiler can be used to produce the layout of any digital circuit in MAGIC. However, when it comes to implementing analog circuits, the layout has to be done manually. It must be mentioned here, that more than 90% of the time is spent in preparing the layout. It becomes important therefore to make the structure highly modular, so as to facilitate the layout. By using identical delays, and identical multipliers, we are able to achieve this objective. Only one mask of a unit delay can be used to produce any number of delays. A single mask of the multiplier can be used to produce any number of multipliers. The entire structure is highly suitable for VLSI implementation. Also, the architecture

could be easily extended to obtain a filter of any order. Once the layout is prepared, the circuit is extracted from the layout and simulated using CaZM.

4.8 Main features of the design

The system described here is a programmable SC FIR filter, the main feature of which is its ability to accept analog as well as digital signals. All op amps in the circuit operate with their non-inverting terminals grounded. The effects of parasitic capacitances are *minimized*. The entire system needs only a two-phased clock for its operation. The input signal need not be binary or N -ary as is the requirement in several other designs [16, 17, 18]. On the other hand, any continuous analog signal can be processed. This SC filter is as flexible as its digital counterpart. The disadvantage is the noise caused by the switches and the quantization of the coefficients which affects the overall response of the filter.

4.9 Results and Discussion

In this section we present and discuss the simulation results of the programmable SC FIR filter. An eighth and a sixteenth order low pass filters were constructed based on the given architecture. The building blocks described in the previous sections were used to construct the filter. The coefficients of the filter were obtained using the Remez exchange algorithm. They were first multiplied by the order of the filter

and were then programmed into the filter. Figures 4.15 and 4.16 show the IC layout of the 8th and 16th order filters respectively. In order to maintain reduced chip area and also reduced costs, we connected all the switches of the multipliers to a single supply pin. We verified the performance of the filters by applying an impulse to the input and observing the impulse response. The impulse response in each case is shown in Figures 4.17 4.18 4.19 and 4.20 and 4.21 respectively. It is found that while the response of the 8th order filter is close to ideal, the 16th order shows a marked deviation in the stop-band. In fact, the stop-band attenuation deviates by 40dB from the ideal. Figure 4.26 shows the close-up of the pass band. It was found that at a frequency of 0.2 of the normalized frequency, which corresponds to 795Hz, the simulated gain is $-0.92dB$ as against a theoretical value of $-1dB$, which corresponds to a gain error of 8%. The deviation from the ideal is due to the parasitic capacitance of the top plate of the capacitor, and the parasitic capacitances of the switch, which have an effect on the smaller coefficients. The delicate combination of coefficients in the stop-band are generally affected, and this effect is magnified for filters of large length ($N = 16$ or more). Larger unit capacitors can be used to overcome this problem. However it leads to a larger area requirement and correspondingly, higher costs. Another reason for the inaccuracy is the capacitor mismatch in the final two-input adder. This again, can be overcome by using large capacitances.

The impulse response of the eighth order filter is shown in Figure 4.17. Here v_1 and v_2 represent the first and second stages of the delay line respectively. Table

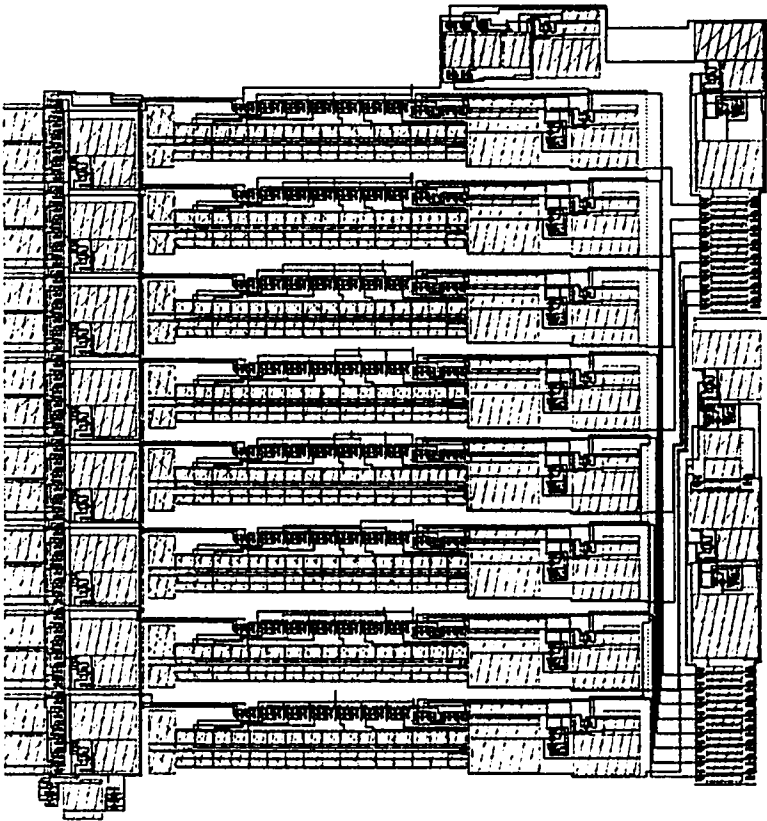


Figure 4.15: IC layout of 8th order SC FIR filter ($area = 3685 \times 3530 \mu m^2$)

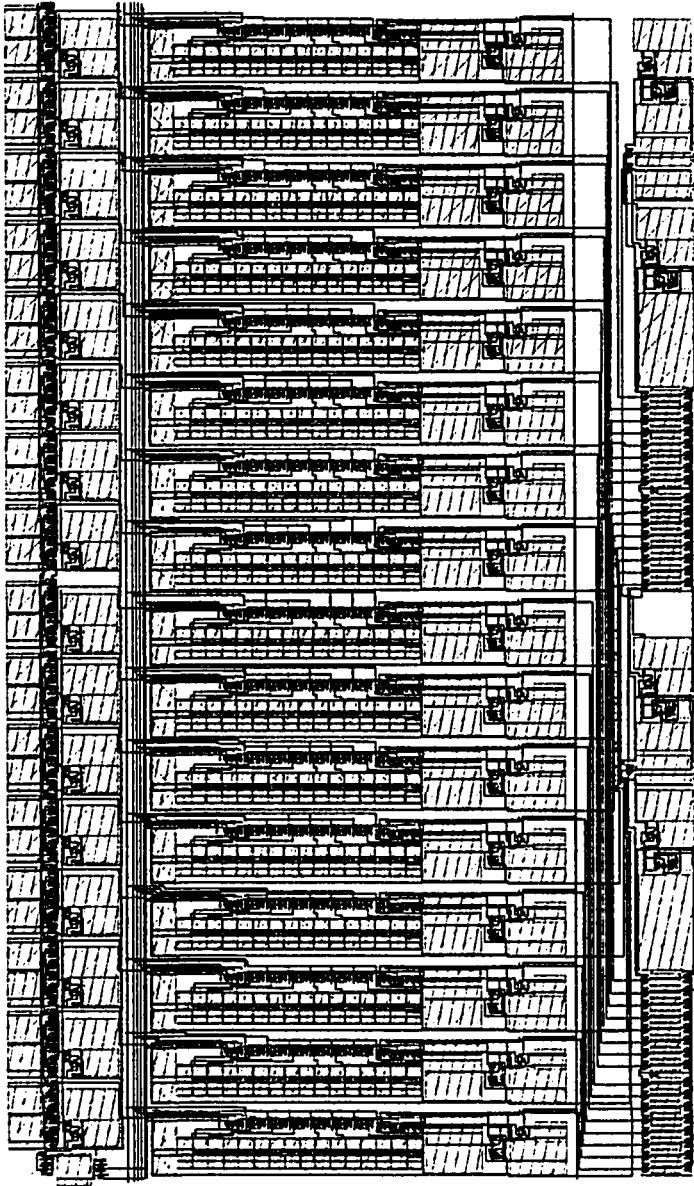


Figure 4.16: IC layout of 16th order SC FIR filter ($area = 6 \times 4mm^2$)

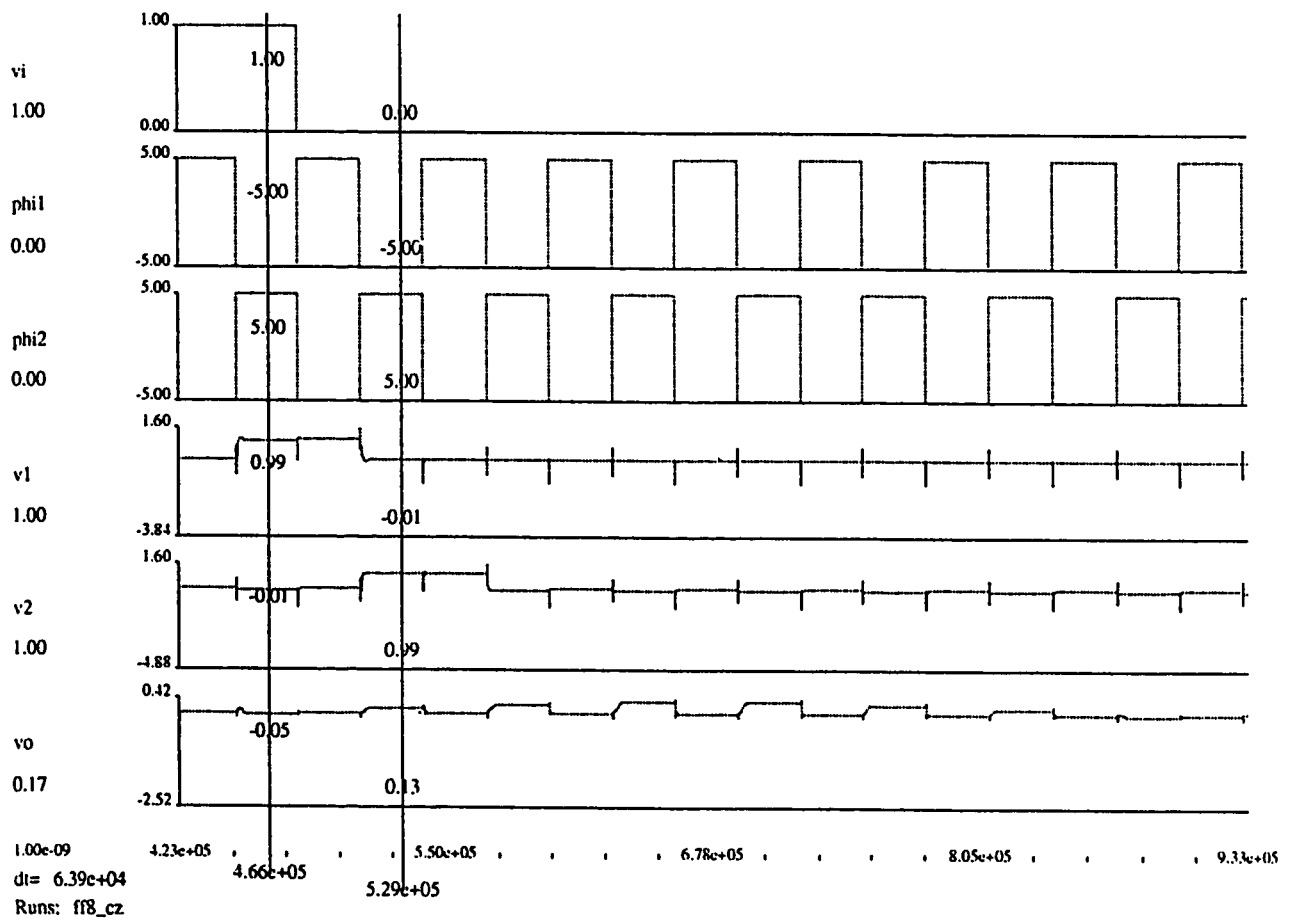


Figure 4.17: 8th order filter: simulation of the impulse response

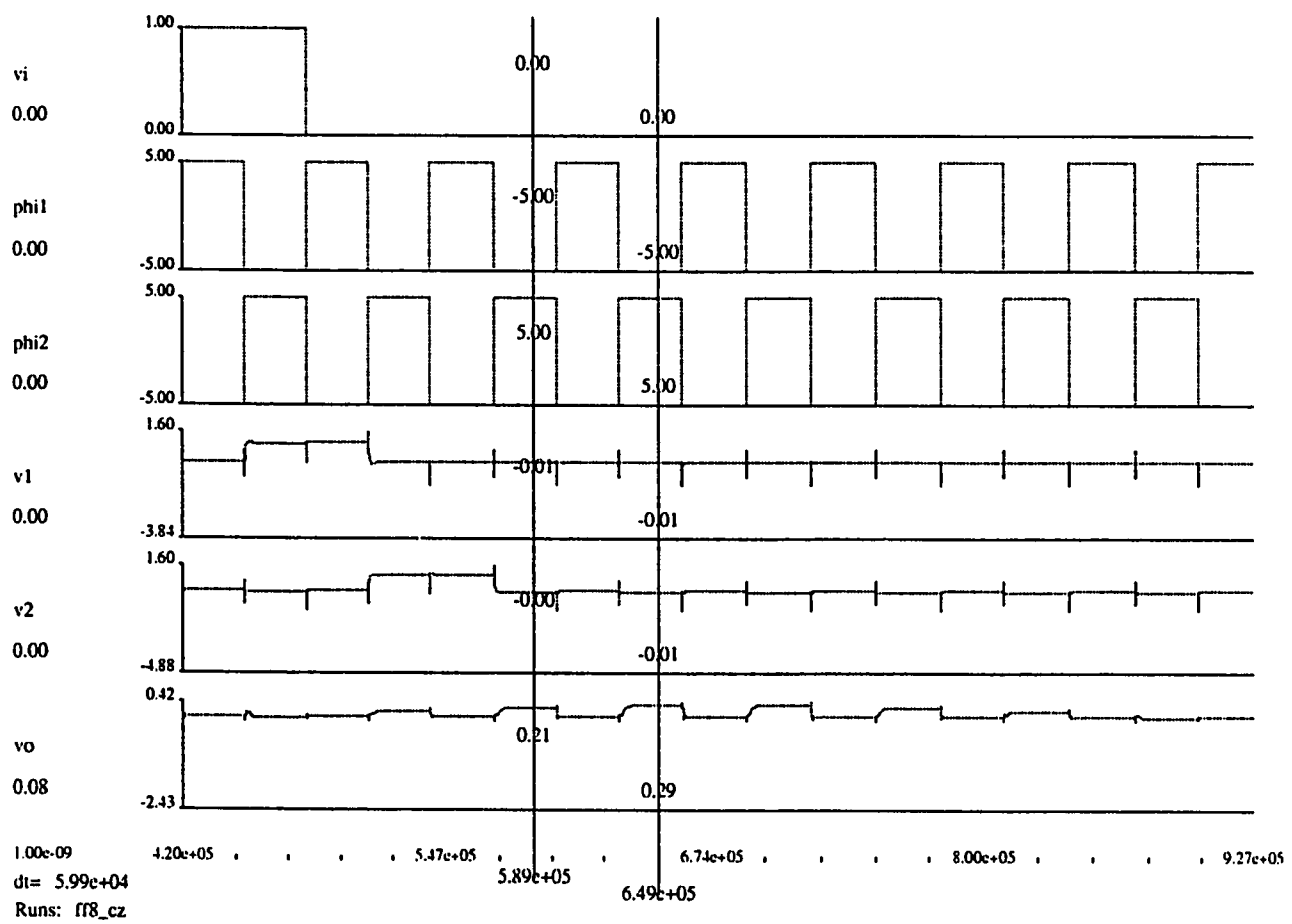


Figure 4.18: 8th order filter: simulation of the impulse response

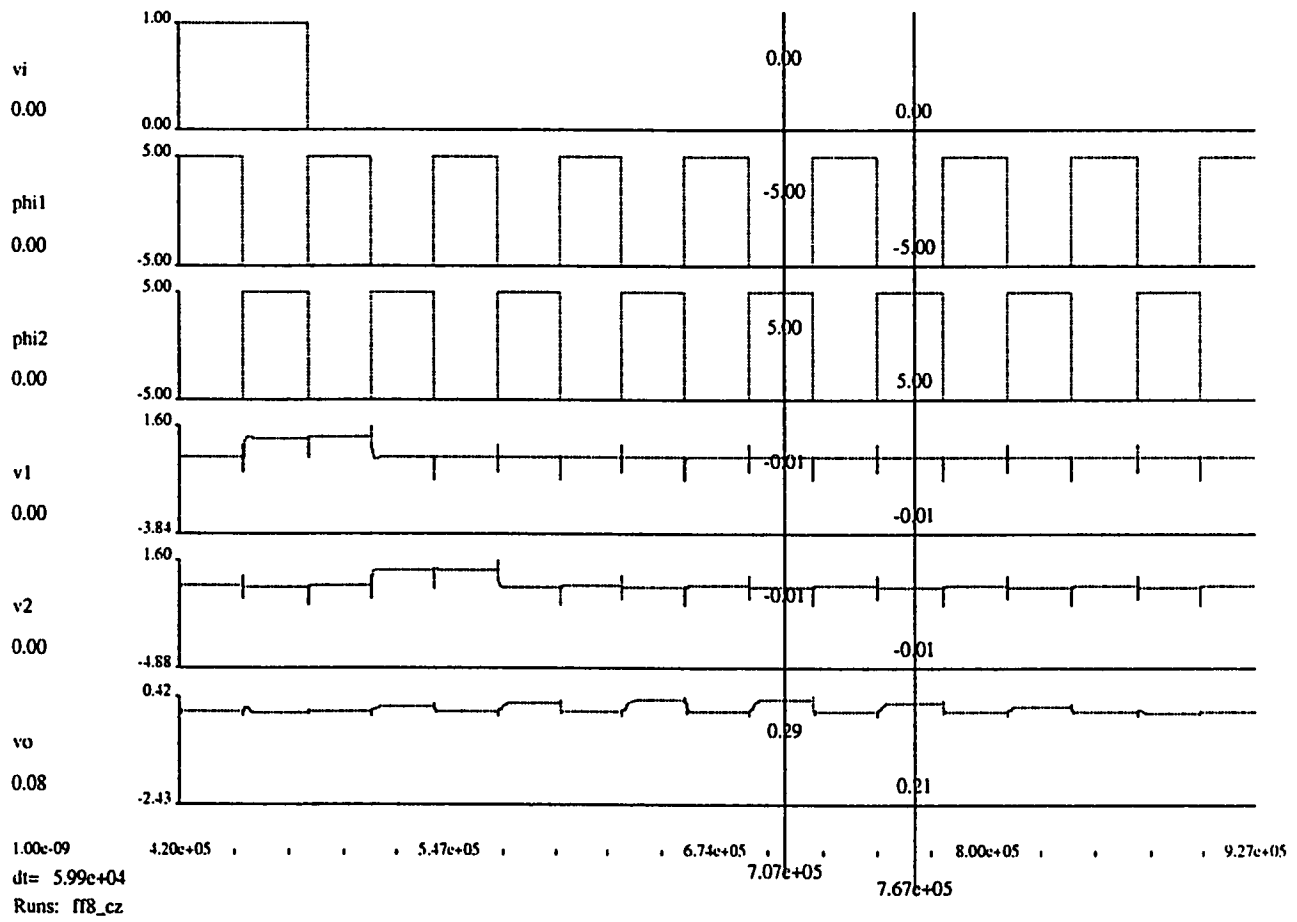


Figure 4.19: 8th order filter: simulation of the impulse response

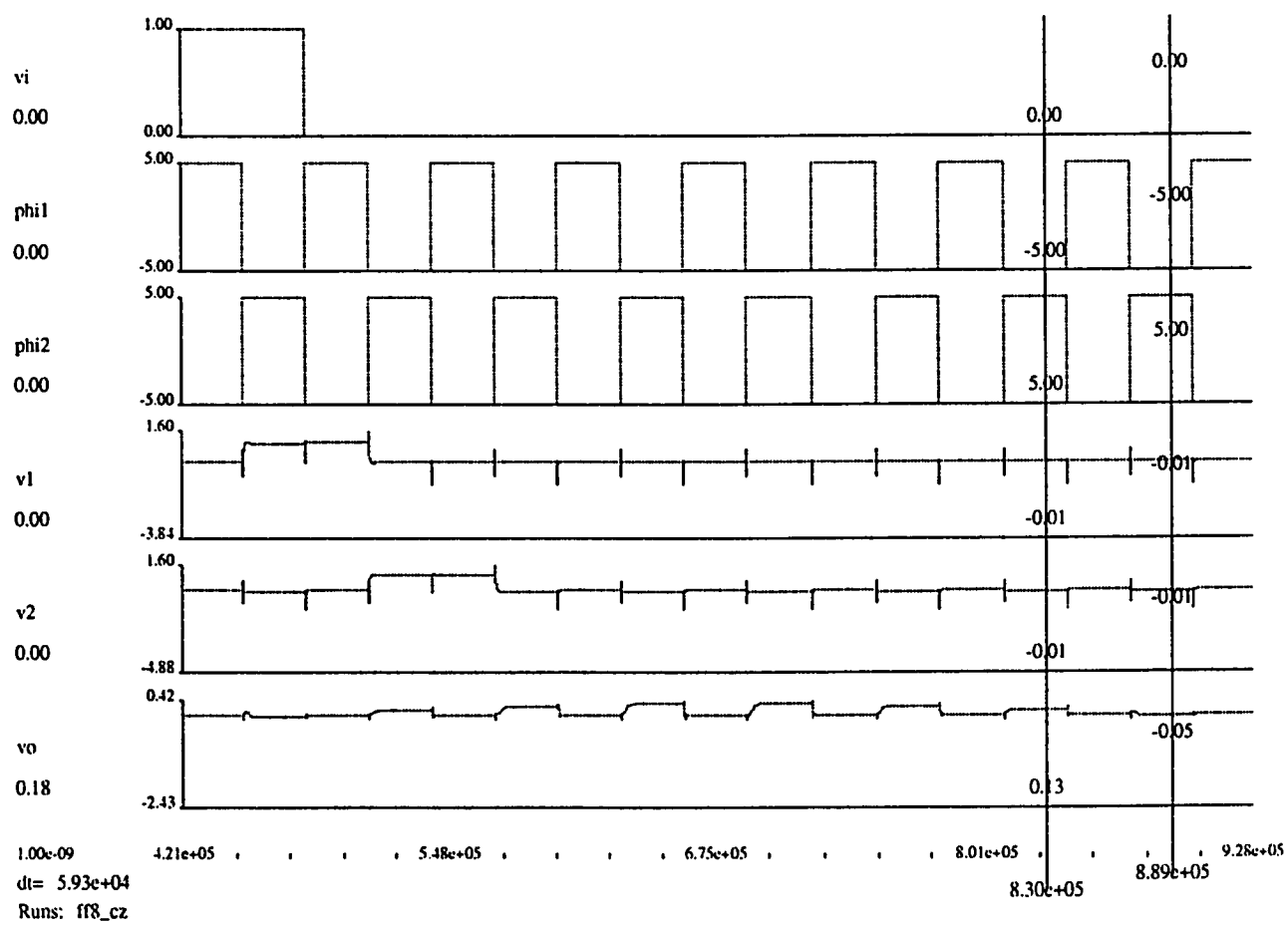


Figure 4.20: 8th order filter: simulation of the impulse response

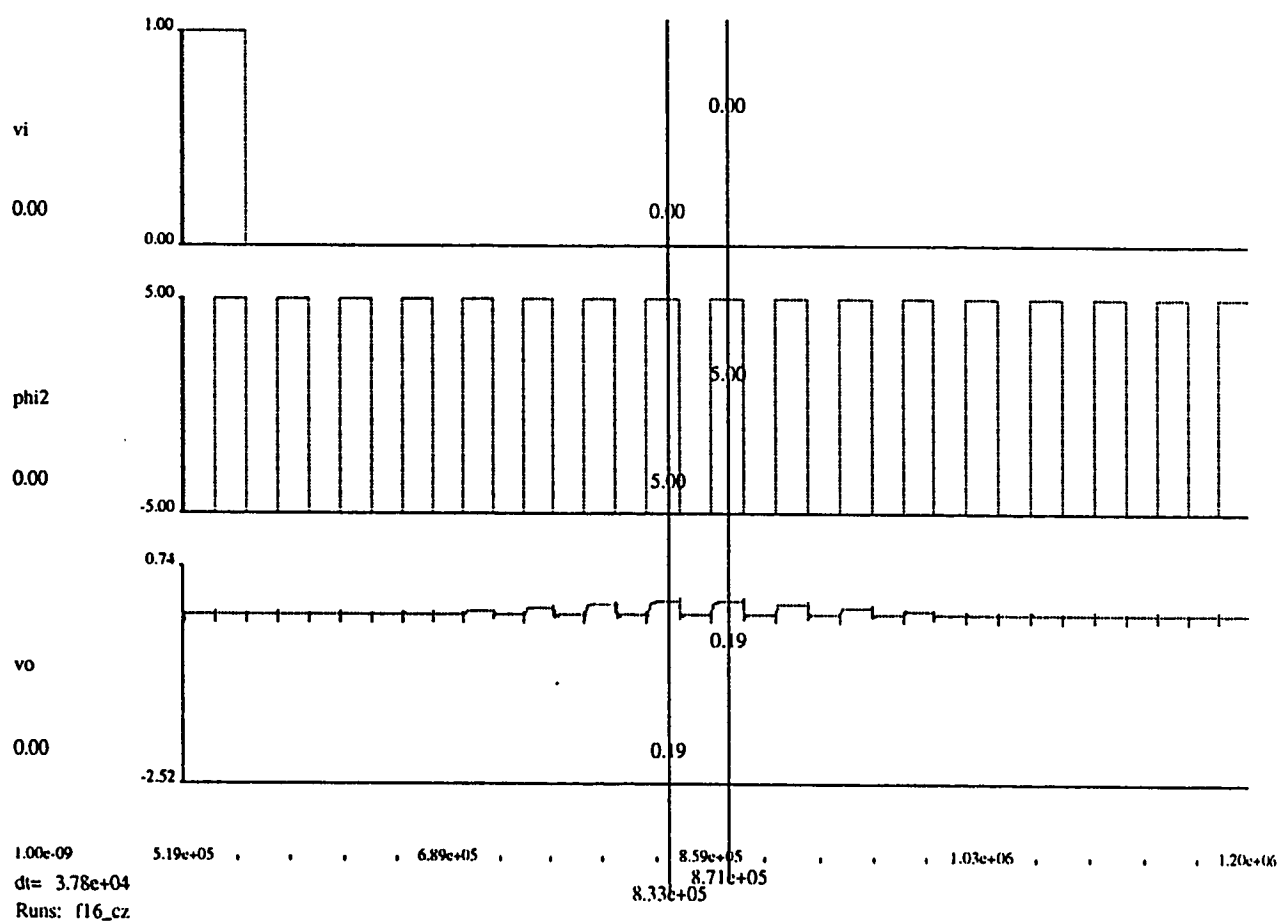


Figure 4.21: 16th order filter: impulse response

Impulse response	Ideal values	Programmed values	Simulated values
h(0)	-0.0636	-0.0625	-.05
h(1)	0.10439	0.1093	0.13
h(2)	0.21265	0.2188	0.21
h(3)	0.29943	0.2968	0.29
h(4)	0.29943	0.2968	0.29
h(5)	0.21265	0.2188	0.21
h(6)	0.10439	0.1093	0.13
h(7)	-0.0636	-0.0625	-.05

Table 4.3: Impulse response of the eighth-order filter

4.3 shows the simulation results of the filter. The impulse response was used to obtain the frequency response of the filter. Figures 4.22 4.23 4.26 and 4.25 show the frequency response of the filters.

A digital input of 1100 was applied to the 8th order filter. The output is shown in Figure 4.24 and also in Table 4.4. The average power dissipation was also measured for the 16th order SC filter at a frequency of 25KHz and was measured as 0.20W.

4.10 Conclusion

In this chapter, we presented the complete design of a programmable SC FIR filter. The chapter began by describing the architecture of the digital filter. The various building blocks in the architecture were replaced by appropriate SC circuits. Some configurations of the delay line were studied, and the one most suitable for the application was selected and implemented. The simulation results were presented, the

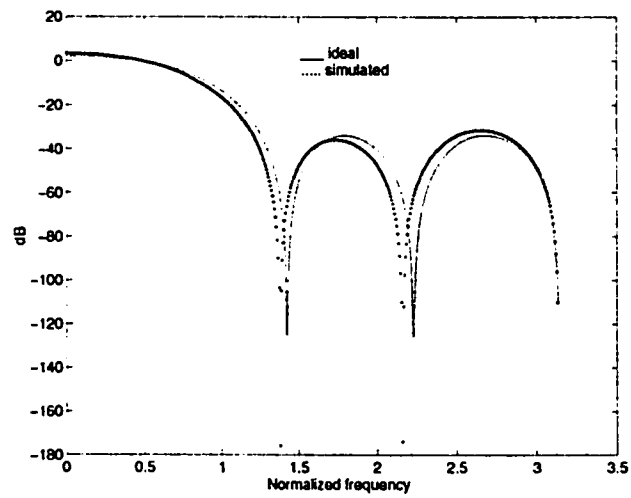


Figure 4.22: Transfer function of the eighth-order SC FIR filter

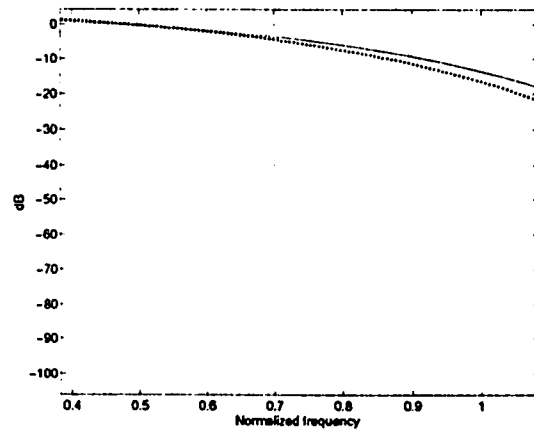


Figure 4.23: Transfer function of the eighth-order SC FIR filter

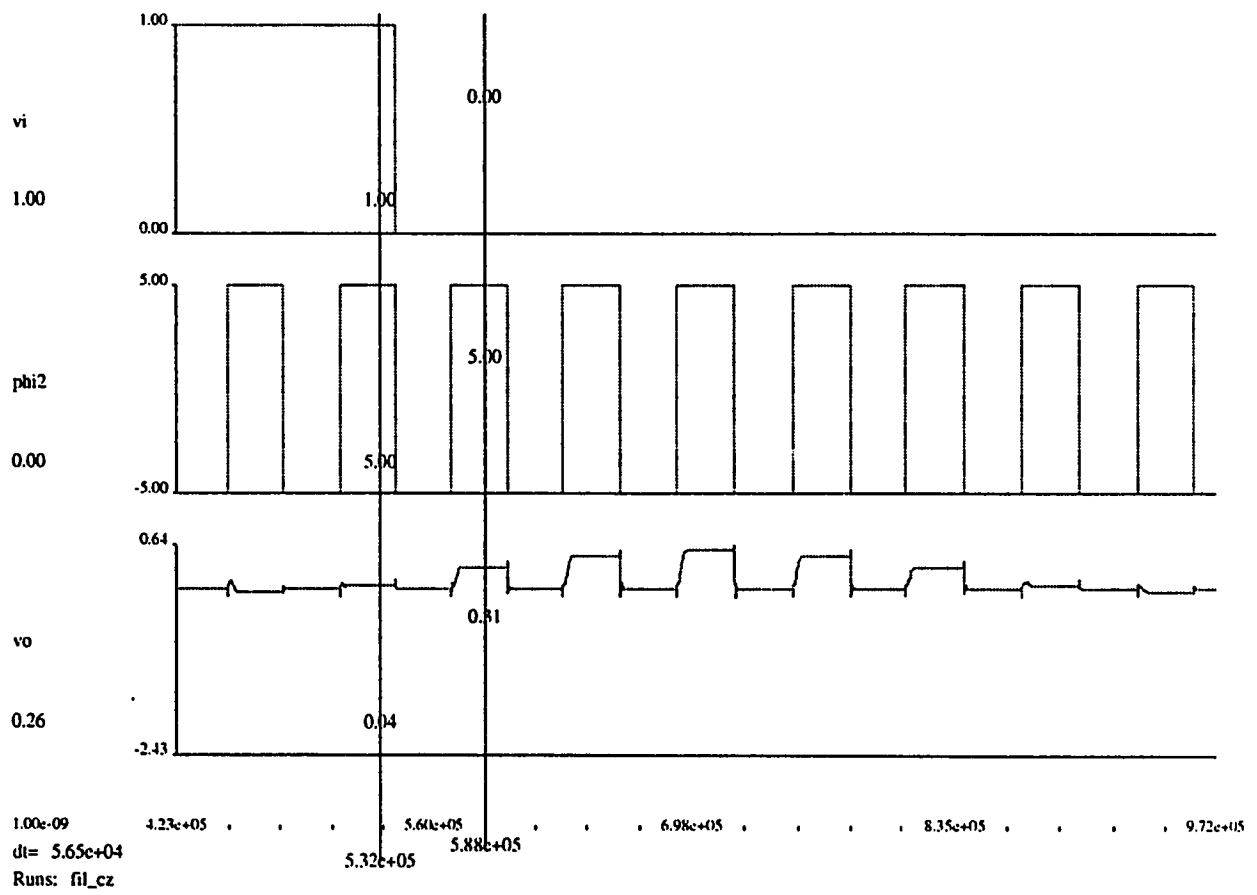


Figure 4.24: 8th order filter: Response due to a digital input 1100

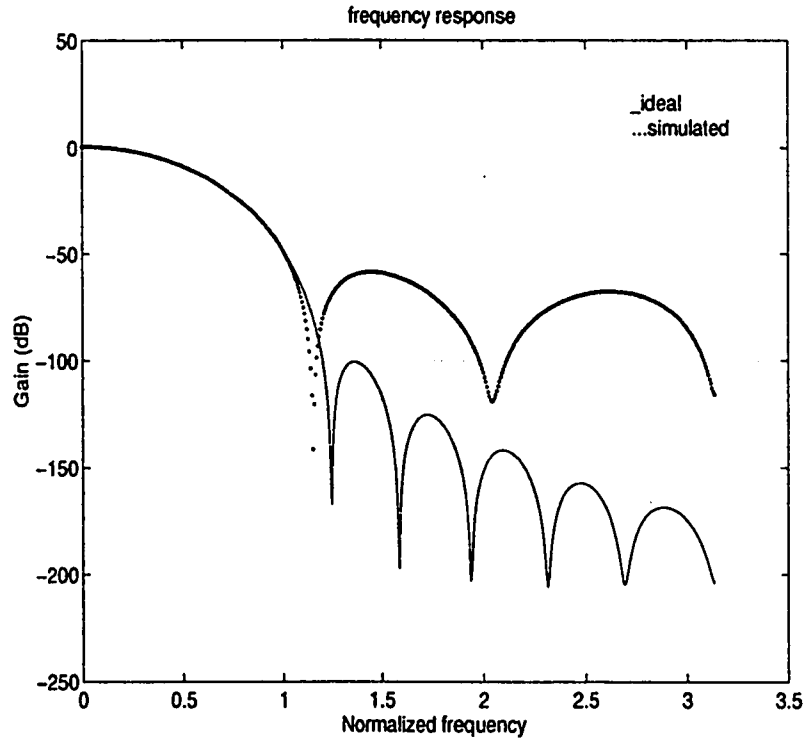


Figure 4.25: Transfer function of the 16th order filter

Pulse No.	Ideal values	Expected values	Simulated values
1	$h(0)$	-0.0636	-0.05
2	$h(0)+h(1)$	0.040	0.04
3	$h(1)+h(2)$	0.316	0.31
4	$h(2)+h(3)$	0.511	0.48
5	$h(3)+h(4)$	0.588	0.56
6	$h(4)+h(5)$	0.511	0.48
7	$h(5)+h(6)$	0.316	0.31
8	$h(6)+h(7)$	0.04	0.04
9	$h(7)$	-0.063	-0.05

Table 4.4: Response due to a digital input 1100

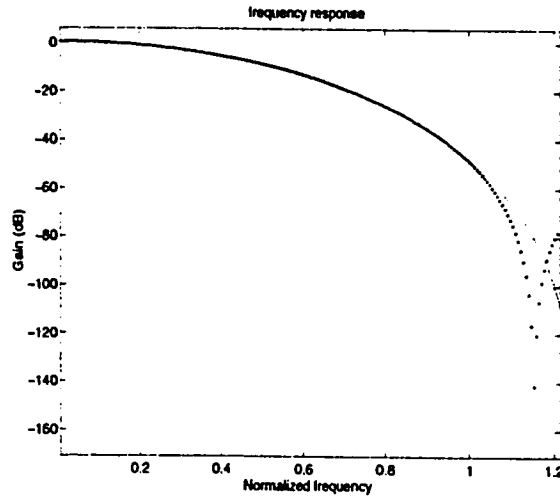


Figure 4.26: 16th order filter: close-up of pass-band

causes of imperfections were analyzed and some suggestions were given to optimize the performance. We next described the multiplying and adding circuits and replaced them by SC units with an emphasis on stray insensitive design. We found that all the basic blocks had a satisfactory performance.

These basic blocks were put together to construct an 8th and a 16th order filter. The simulation results in each case were presented and discussed. The chapter also highlighted the main feature of the design, namely the *stray insensitive nature* and the completely *parallel* structure which is suitable for VLSI implementation.

Chapter 5

Conclusion

In this thesis we presented a programmable SC FIR filter with the same architecture as that of a digital filter. Since no assumption was made on the type of input signal to be processed, the filter can process binary, N -ary as well as analog signals. In other words, the filter has all the advantages of a DSP system, in addition to being able to process an analog signal. The versatility of the architecture lies in the fact that any desired filter specifications can be met while using the same filter structure.

This thesis was based on the work done in [22] where a 4th order SC FIR filter was designed and implemented. It was found that the delay line in the filter was the major source of error in the system. Hence a superior delay line configuration was used and we were able to obtain an eighth order filter with an improved performance.

We then extended this work to the 16th order case and found that the parasitic capacitances associated with the top plate of the capacitor, and the random offset

voltage of the op amp limit the performance. Their effect is especially noticeable for filters of large length.

The architecture presented, although a very attractive tool for signal processing applications, can be used for relatively small order systems. We are convinced that a 12th order system would make a reasonable limit for high precision applications.

Appendix A

Model Parameters

```
*****
** **
** ( MODEL M125CN ) **
** **
** LEVEL II MOSFET PARAMETERS **
** MCNC 1.25 CMOS PROCESS **
** ( NOMINAL ) **
** **
*****
```

```
.model nenh nmos
```

```
+   Level=2           Ld=0.0u           Tox=225.000e-10
+   Nsub=1.066e+16     Vto=0.622490      Kn=5.138000E-05
+   Gamma=.639243      Phi=.31           Uo=1215.74
+   Uexp=4.612355e-2   Ucrit=174667      Delta=0.0
+   Vmax=177269        Xj=.9u           Lambda=0.01
+   Nfs=4.55168e+12    Neff=4.68830      Nss=3.000000E+10
+   Tpg=1.00000        Rsh=60           Cgso=2.89e-10
+   Cgdo=2.89e-10      Cj=3.27e-04      Mj=1.067
+   Cjsw=1.74e-10      Mjsw=.195
```

```
.model penh pmos
```

```
+   Level=2           Ld=.03000000u      Tox=225.000e-10
+   Nsub=6.575441e+16  Vto=-0.63025      Kp=2.400000E-05
+   Gamma=0.618101     Phi=.541111      Uo=361.941
+   Uexp=8.886957e-02  Ucrit=637449      Delta=0.0
+   Vmax=63253.3       Xj=0.112799u      Lambda=0.02
+   Nfs=1.668437e+11    Neff=0.64354      Nss=3.000000E+10
+   Tpg=-1.00000       Rsh=150           Cgso=3.35e-10
+   Cgdo=3.35e-10      Cj=4.75e-04      Mj=.341
+   Cjsw=2.23e-10      Mjsw=.307
```

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